Service Manual

Tektronix

671-0058-XX
MPU Board

070-7413-03

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The main power disconnect is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition. CSA Certification includes the equipment plus those power cords appropriate for use on the North America power network. All other power cords supplied are approved for the country of use.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power up the instrument until such objects have been removed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury or damage to the product, do not operate this product with covers or panels removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

Only qualified personnel should perform service procedures. This Service Safety Summary and the General Safety Summary should be read before performing service procedures.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

To avoid personal injury from high current, remove jewelry such as rings, watches, and other metallic objects, before servicing the instrument. Do not touch exposed connections and components while power is on. Disconnect power before soldering, removing protective panels, or replacing components.

USE CAUTION WHEN SERVICING THE CRT

The CRT assembly should be replaced only by qualified personnel familiar with CRT servicing procedures and precautions. CRTs retain hazardous voltages for long periods of time after power-down. Before attempting any work inside the monitor, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode. Use extreme caution when handling the CRT, rough handling may cause it to implode. Do not nick or scratch the glass or subject it to undue pressure during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

Section 1
GENERAL INFORMATION

ABOUT THIS MANUAL

This manual contains service information for the MPU board used in the PRISM 3000 Series or the 2500 Series TestLab mainframes. The MPU board is a single-board host computer that provides central control and memory for a signal analyzing system.

There are two versions of the MPU board. One version is used in the PRISM 3002 and the 2510 TestLab mainframes and has a Tektronix part number of 671-0058-00 through 671-0058-1X. The other version is used in the PRISM 3001 and 2505 TestLab mainframes and has a Tektronix part number of 671-0058-5X. The two versions are similar in circuitry and in operation. The differences involve mechanical and connector changes needed to install the board in the different mainframes.

This manual explains how to verify, service, troubleshoot, and repair the MPU board. It is written with the assumption that the MPU board is installed in a signal analyzer mainframe. The following is a brief description of manual contents.

Section 1, *General Information*, describes related manuals and provides a brief description of the MPU board and related modules.

Section 2, *Specifications,* describes the functional characteristics and the performance requirements (with supplemental information) of the MPU board.

Section 3, *Connectors and Cabling,* describes electrical connectors and test points associated with the MPU board. Also provided are illustrations that show the pin/signal assignments for the microprocessor and each gate array integrated circuit.

Section 4, *Theory of Operation,* provides descriptions of MPU board circuit operation.

Section 5, *Verification and Adjustments*, describes how to verify the performance of the MPU board and how to perform adjustments.

Section 6, *Disassembly/Installation*, explains where to locate MPU board removal/replacement procedures.

Section 7, *Maintenance,* describes how to perform needed maintenance on the MPU board.

Section 8, *Troubleshooting*, describes general troubleshooting procedures and power-on diagnostics.

Section 9, *System Diagnostics Software*, describes how to use the diagnostic software to perform system verification and component-level troubleshooting. Also provided are detailed descriptions and index troubleshooting information for each diagnostic routine for the MPU board and related modules.

Section 10, *Electrical Parts List*, lists all the replaceable electrical parts and their part numbers associated with the MPU board. Parts for modules supported with separate service manuals are not included.

Section 11, *Diagrams,* contains block diagrams and schematics for the MPU board.

Section 12, *Mechanical Parts List*, lists the replaceable mechanical parts and their part numbers for the MPU board.

Section 13, *Signal Descriptions*, describes the major functional signals of the MPU and related modules.

Appendix A, *Kernel Test Monitor,* describes tests that can be used to perform low-level troubleshooting of MPU compute kernel circuitry.

RELATED MANUALS

Service information for a signal analyzer system is contained in several different service manuals. Thus, a service manual package and service kit accessories will vary depending on the particular mainframe and installed acquisition modules. Providing the service information in this manner minimizes duplication and aids retrieval of service information. Service information is contained in the following types of service manuals.

Mainframe Service Manuals

These manuals provide service information for the different mainframe mechanical enclosures and associated chassis-mounted components. Mainframe service manuals also contain service information for system peripherals; such as, keyboard and operator console, power supplies, floppy disk drive, hard disk controller and drive, and display units. Signal interconnect drawings are also provided.

Acquisition Module Service Manuals

A mainframe can contain any of several different acquisition modules. Each acquisition module is supported with its own service manual. Content of these service manuals is similar to the content of the MPU board service manual.

MPU Board Service Manual

Refer to *Manual Contents* earlier in this section for detailed contents of this manual.

Test Fixture Service Manuals

Special test fixtures are available to aid low-level servicing of the MPU board and some signal acquisition boards. Instruction manuals describe how to use and service this special test equipment.

How to Order Manuals

Manuals not shipped as a standard accessory with your product may be ordered individually. Contact your Tektronix representative for a complete list of related manuals and service kits for your particular mainframe configuration.

MPU BOARD GENERAL DESCRIPTION

The following is a brief description of the MPU hardware and operating system. (See Figure 1-1.)

MPU Board Hardware

The MPU board is a single-board host computer that provides central control and memory for an instrumentation system. It is based on a Motorola 68010 microprocessor, 2 Mbyte or 4 Mbyte RAM, and 64 Kbyte boot ROM.

The MPU board provides a modified RS-232 port for keyboard communications and a standard RS-232-C port for host communications. It also provides a generic Tektronix 1200-Series COMM Pack port for RS-232-C, GPIB, and printer interfacing. A 640 X 400, non-interlaced display output provides connection for an external monitor. A hard disk drive (optional for the PRISM 3001 Series mainframes) is connected to the MPU board for mass storage.

All application modules within a Mainframe system connect to either the MPU board or an Expansion board via TekLink cabling. Service information for the Expansion board is located in the *PRISM 3002 Series Mainframes and 2510 TestLab Mainframe Service Manual.*

Refer to *Section 4: Theory of Operation* in this manual for detailed descriptions of MPU board circuit operation.

MPU Board System Software

System software is based on a real-time operating system (pSOS). The MS-DOS compatible file system is optimized for use in an instrumentation environment. A full set of general-purpose utilities supports the menu-based user interface. Basic external communications software provides instrument control and transfer of binary information. Comprehensive diagnostic software supports both automatic power-on tests and menu-driven self-tests.

RELATED MODULES

The modules used in a mainframe depend on the specific PRISM 3000 Series or 2500 Series TestLab mainframe and its optional modules. The following is a brief description of each electrical module that can be connected to an MPU board. These modules are described in detail in other service manuals. Refer to *Related Manuals* earlier in this section for the type of service manuals available and for ordering information. Figure 1-1 illustrates the hardware configuration capabilities of the MPU board.

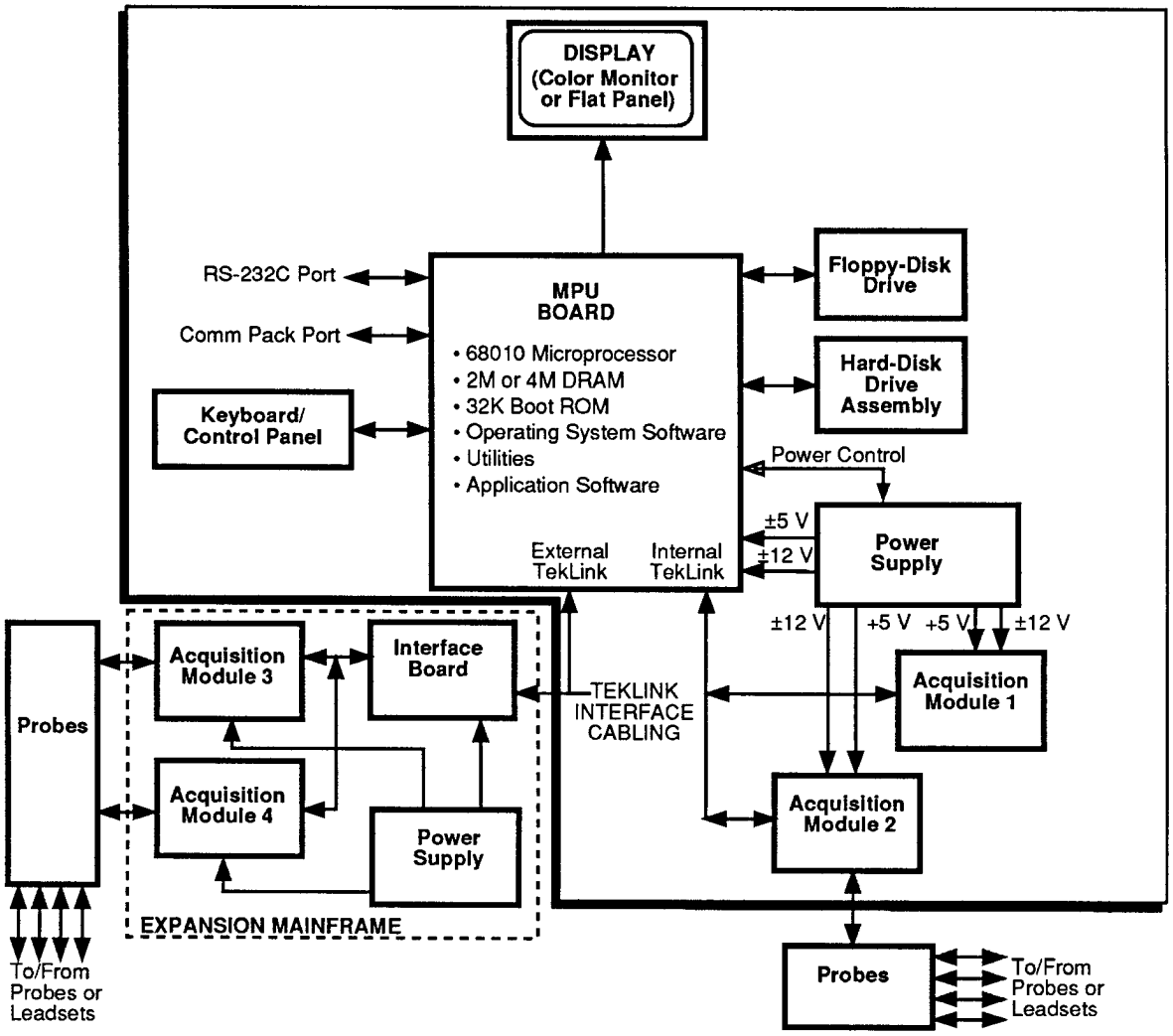


Figure 1-1. MPU board and associated mainframe modules.

Control Panel (Keyboard)

Whether a keyboard or a control panel is used depends on the mainframe in which the MPU board is installed. A control panel can consist of software-programmable function keys, cursor-control keys, a hex key pad, and a Select control knob. Some control panels also include a standard QWERTY keyboard. The function keys are assigned special functions by the operating system or the application software (depending on which acquisition modules are installed). You can use functions keys to control data acquisition and display windowing. You can use the knob to make menu selections. Refer to the applicable mainframe service manual for details regarding the specific keyboard or control panel used with your mainframe.

Display Unit

The MPU board provides a 640 X 400 pixel, non-interlaced display output to drive either a color CRT monitor, a monochrome CRT monitor, or a flat-panel display. Characters are displayed using a programmable character set (8 X 10 cell with full descenders and underlining). Normal and inverse video are provided. Color attributes can be specified.

Bit-mapped graphics are supported. Character and graphics data can be displayed in either one or two windows. The contents of a window are smooth-scrolled, both vertically and horizontally.

Acquisition Modules

Acquisition modules interface to the MPU board through special interface hardware and communications protocol (TekLink). Separate, but functionally identical, links are provided by an MPU board for internal and external acquisition modules. Internal acquisition modules reside in Mainframe configurations that contain an MPU board. One or two external acquisition modules may reside in an Expansion Mainframe (PRISM 3000 Series only) and connect to the MPU board using external TekLink cabling. Service information for acquisition modules is documented in separate service manuals. See *Related Manuals* earlier in this section for the type of service manuals available and for ordering information.

Floppy Disk Drive

A 3.5 inch, hard-shell disk drive provides storage for the operating system, diagnostics, applications software, and acquisition data files.

Hard Disk Drive

A hard disk drive (optional in the PRISM 3001 mainframes) provides mass storage for system and application software. The hard disk drive is supported by a Hard Disk Controller board for the ST506/412-interface hard disk drives or by a IDE Interface board for the IDE-interface hard disk drives. These boards provide interfacing between the MPU board and the hard disk drive.

Expansion Board

An Expansion board is mounted in a 3002E Expansion mainframe in the same area as the MPU board in a system mainframe. Its purpose is to interface one or two acquisition modules in the expansion mainframe to the MPU board in system mainframe via external TekLink cabling.

Power Supplies

All mainframes contain a power supply. The specific power supply used depends on the type of mainframe. The power supply provides +12 VDC, +5 VDC and -12 VDC to the MPU board and acquisition modules. Power for all other system peripherals is routed by, and fused on, the MPU board.

Probe Modules and Lead Sets

Different probe modules are available for connecting an acquisition module to the system under test (SUT). The probe module used depends on the physical requirements of the circuity to be observed or tested. A probe module uses a lead set to physically connect the probe to the system under test. Again, different lead sets are available depending on the specific probe and physical requirements of the system to be observed or tested.

Section 2
SPECIFICATION

This section lists two types of specifications: (1) those that are classified as environmental, physical, or "static" specifications (specifications that cannot be verified by the user); and (2) those that are actual operational parameters (specifications that are user verifiable). Refer to the Verification and Adjustment procedures in Section 5 for procedures that verify the performance specifications.

The following terms are used in the specification tables:

- *Characteristic:* A property of the product.
- *Performance Requirement:* The primary performance characteristics of the product that can be verified using verification procedures.
- *Supplemental Information:* Statements that describe typical performance for characteristics of secondary importance (those that are not usually verified using verification procedures), or statements that further explain related performance requirements.

CHARACTERISTICS/SPECIFICATIONS

The performance characteristics in this section are valid under the following conditions:

1. The MPU board must be operating in an environment as specified in Table 2-1 in the applicable mainframe service manual.
2. You must allow at least a 20 minute warm-up period before starting the verification/operational procedures.

The following tables list the specifications and performance characteristics of the Mainframes:

Table 2-1
MPU Functional Requirements

Characteristic	Description
Kernel	
CPU	Motorola 68010
RAM	2 Mbyte or 4 Mbyte
ROM	32 Kbit x 16
Clock Calendar	Programmable: Day, Month, Time
Oscillator	32.7876 kHz ±0.006%
Battery (Calendar)	
Type	Lithium BR2325, 3 V, 0.15 Ah
Life	1 to 5 years
Mass Storage	
Floppy Disk Drive	720 Kbyte (formatted)
Hard Disk Drive (Optional for PRISM 3001 Series)	20 or 40 Mbyte ST506/412 interface 80 Mbyte available for 2505 or 2510 TestLab 64 Mbyte IDE interface 127 Mbyte available for 2505 or 2510 TestLab
Acquisition Module Support (maximum)	4 (2 on "Internal TekLink"; 2 on "External TekLink")
Communication Support	
RS-232-C Port	DTE
Asynchronous mode	Half duplex, full duplex
Baud Rates	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 4800, 7200, 9600, 19200
Driven Lines	TD, RTS, DTR
Monitored Lines	RD, CTS, DSR, DCD, RI
Keyboard Port	19200 Baud, serial data
TekLink Port	12.5 MHz, serial data
1200-Series COMM Pack Port	COMM Packs Supported: 1200C01 RS-232-C 1200C02 GPIB 1200C11 Parallel Printer
Data Path	8 or 16 bits (Pack-dependent)
Address Space	128 Kbytes
Display Port	Supports color or monochrome CRT or Flat Panel Display
Display Controller	Supports EGA Color and monochrome CRTs and Flat Panel
Displays	
Viewable Resolution	640 X 400 pixels
Scrolling	Horizontal and vertical smooth scrolling
Data Windows	2
Cursors	3 per data window
Character Font	8 X 10 pixels
Character Matrix	10 X 16 pixels
Screen Copying	Programmable "pixel-based" reading by CPU permits printing of screen images

(Cont.)

Table 2-1
MPU Functional Requirements (Cont.)

Characteristic	Description
Ext. Trigger Out	50 Ω source impedance
Output Voltage	
High into open load	≥3.8 V
High into 50 Ω load	≥1.9 V
Low	≤0.6 V @ 7 mA
Pulse Width	≥20 ns
Ext. Trigger In	
Input Resistance	1 MΩ ±1%
Input Capacitance	37 pF ±5 pF
Maximum Input Voltage	±20 V
With X1 Probe or 50 Ω Coaxial Cable	
Input Threshold	1.4 V ±100 mV
Pulse Amplitude	≥1.8 V high; ≤0.6 V low
Pulse Width	≥30 ns
With X10 PROBE	
Input Threshold	1.4 V ±500 mV
Pulse Amplitude	≥2.4 V high; ≤0.6 V low
Pulse Width	≥30 ns
Slew Rate	≥5 V/µs

Table 2-2
MPU Performance Requirements

Characteristic	Performance Requirements	Supplemental Information
Master Clock	10 MHz ±0.01%	671–0058–06 and below 671–0058–50 and below
	10.01125 MHz +/– 0.01%	671–0058–07 and above 671–0058–51 and above
TekLink Clocks		
M_CLK, M_CLK/		
Frequency	50 MHz ±0.001%	
Duty Cycle	50% ±0.1%	
Logic level		+5 V ECL referenced to the TekLink supply
S_CLK		
Frequency	12.5 MHz ±0.001%	
Duty Cycle	50% ±0.1%	

Section 3
CONNECTORS AND CABLING

INTRODUCTION

This section shows the signal interconnections for the MPU board. Use this information to trace signal flow between the various electrical modules. Signal information is provided by the following:

- MPU Board Connector Diagram
- Signal Interconnect Diagrams
- Gate Array Pin Configuration and Signal Assignments
- 68010 Microprocessor Pin Configuration and Signal Assignments
- Test Points and Test Connectors

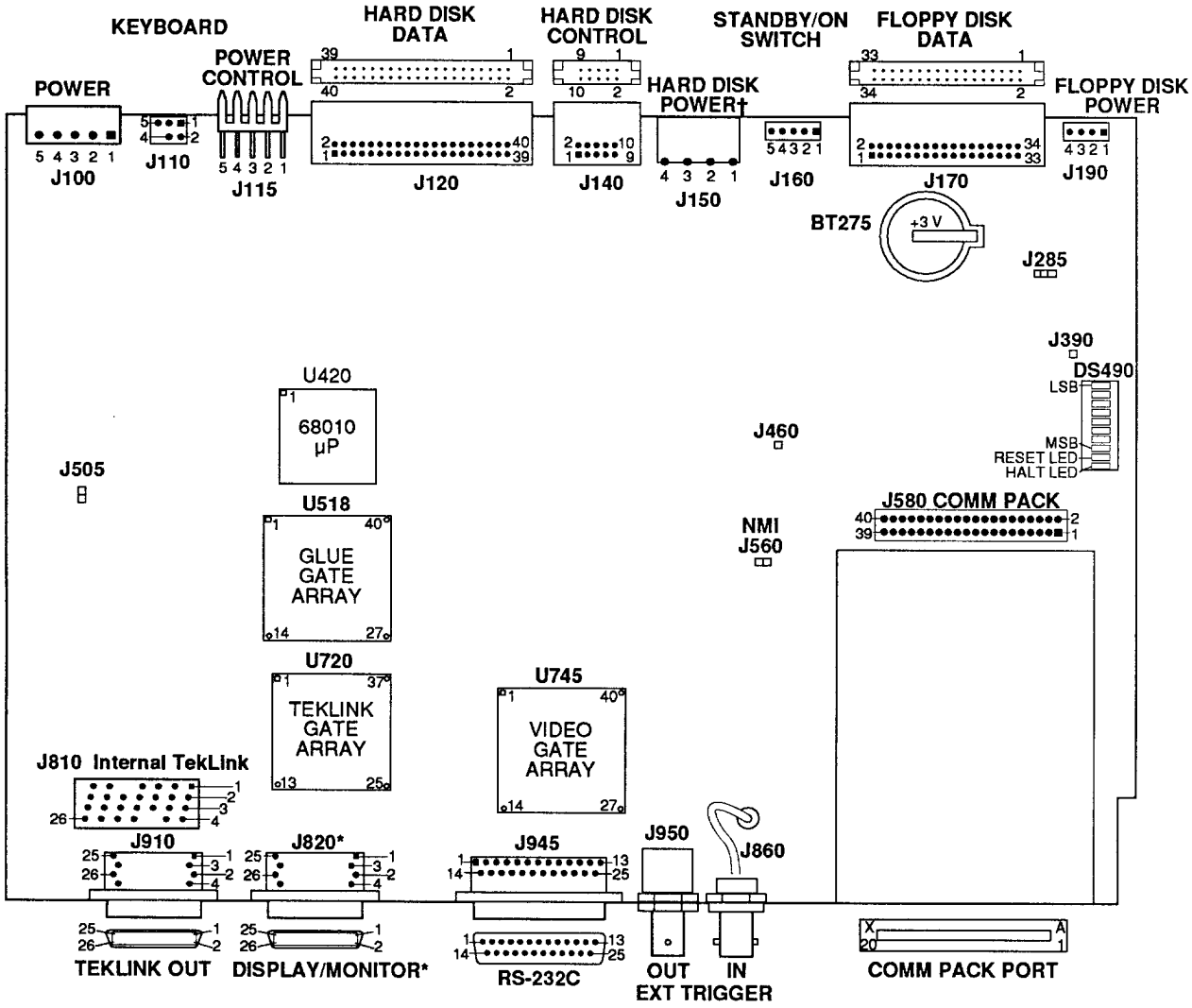
A description of each interconnect signal to/from the MPU board is provided in *Section 13: Glossary*.

MPU BOARD CONNECTOR DIAGRAM

Figure 3-1 shows the location of each connector on the MPU board, with the board viewed component side up. Note that the pin-numbering convention is provided for each connector.

Figure 3-1 illustrates the connector configuration for the version of the MPU board that is used in a PRISM 3002 or 2510 TestLab mainframe. The board is installed in a mainframe in which two application modules can be installed. The mainframe has an external-mounted display or monitor. You can connect the MPU boards to an expansion mainframe using the external TekLink connector. The Display and External TekLink connectors are shown in Figure 3-1.

For the version of the MPU boards that is installed in a PRISM 3001 or 2505 TestLab mainframe, the display is mounted inside the mainframe. This board connects to a single application module inside the mainframe. The internal display and the application module connect to the MPU board via the Connector Adapter board mounted on the solder side of the MPU board. Figure 3-2 shows the connector pin assignments for the Display and TekLink connectors on the Connector Adapter board.



* Not included on MPU board used in PRISM 3001 or 2505 TestLab mainframes.
† Provides Auxillary Fan power in PRISM 3002 mainframes. Not used to provide power to hard disk drive with IDE interface.

Figure 3-1. MPU board connectors and pin keying.

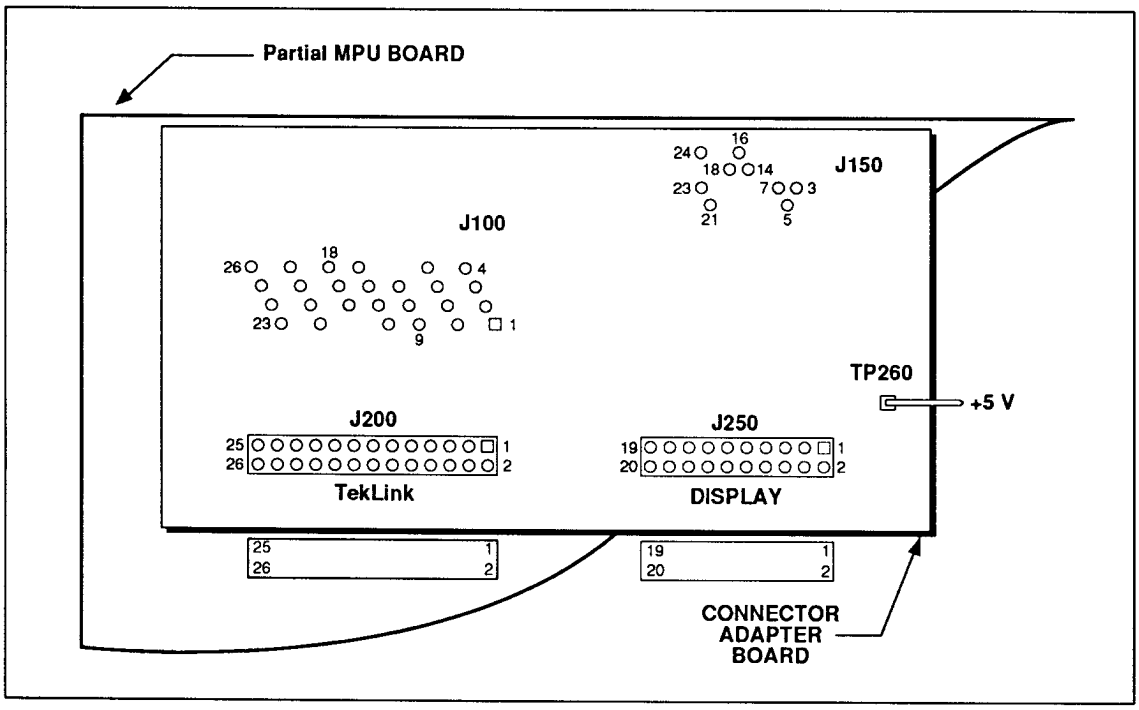


Figure 3-2. Connector Adapter board used in the PRISM 3001 or the 2505 TestLab.

SIGNAL INTERCONNECT DIAGRAMS

Signal interconnect diagrams for each MPU and Mainframe connector are located on pull-out sheets in Section 10 of the applicable mainframe service manual. These diagrams show the signals assigned to each connector pin.

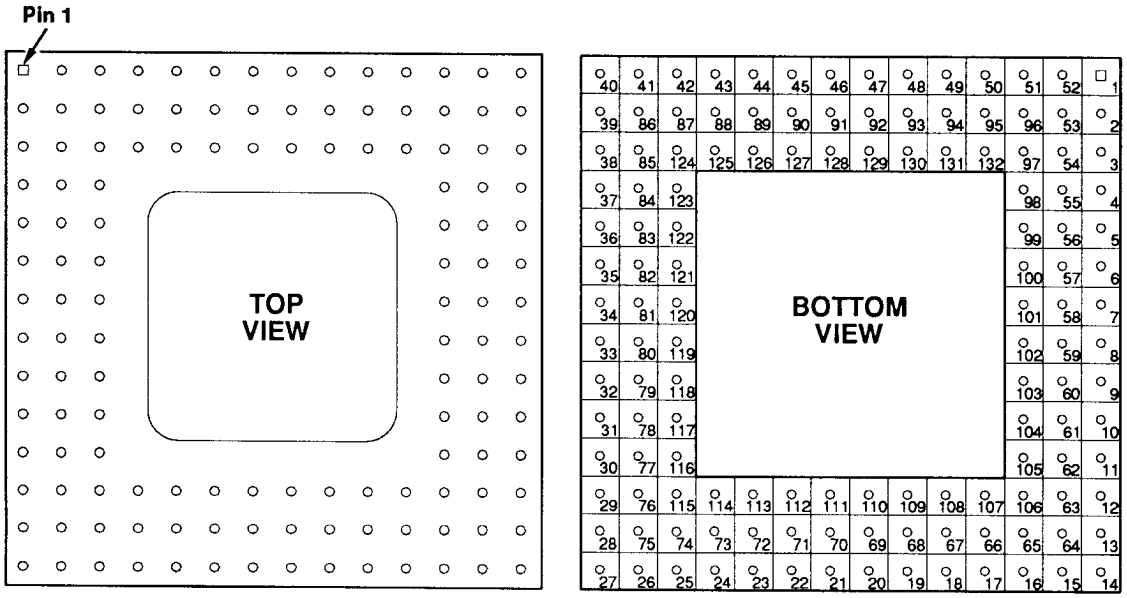
NOTE

Refer to the appropriate mainframe service manual for a complete set of signal interconnect diagrams for your particular instrumentation system.

GATE ARRAY PIN CONFIGURATION AND SIGNALS

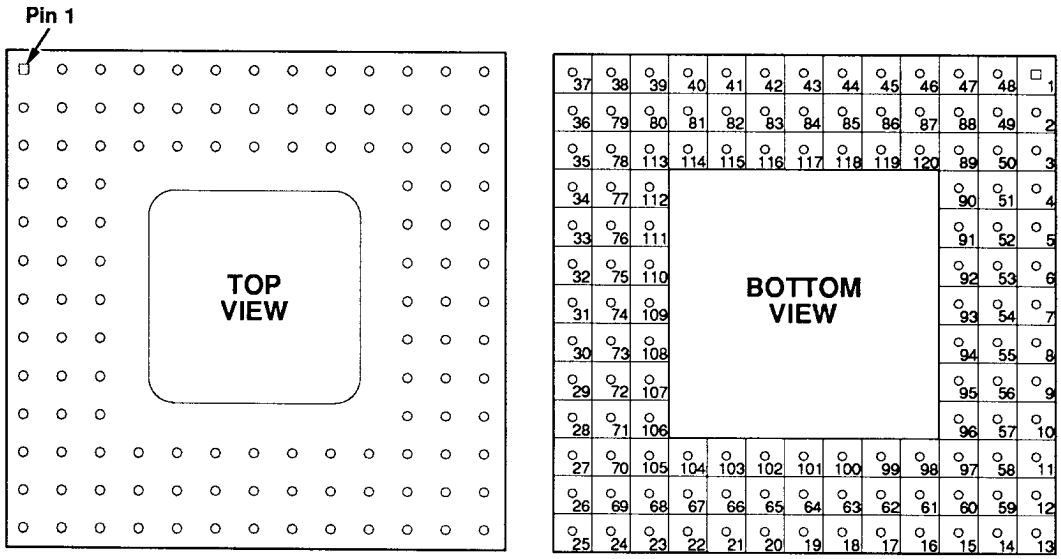
The MPU board includes three gate array integrated circuits; GLUE, TekLink, and Video. Figures 3-3, 3-4, and 3-5 show pin configuration and signal assignments for these gate arrays.

Figure 3-1 shows the location of each array on the MPU board and identifies pin 1 of the array on the component side of the MPU board.



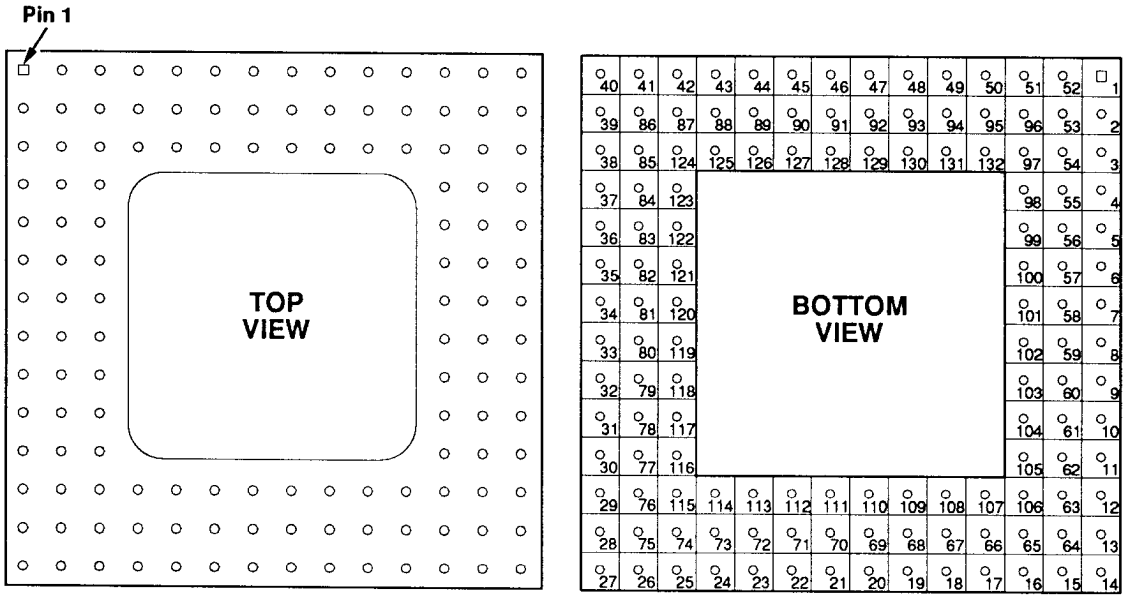
Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	KAS/	28	RID15	55	10MHZ	82	KD10	109	GBA9
2	KD1	29	RMRW	56	KD0	83	KA17	110	GBA1
3	DTACK/	30	LORA8	57	KD6	84	KA20	111	RID2
4	KLDS/	31	LORA5	58	LEDSEL	85	KA19	112	RID5
5	KD2	32	LORA2	59	BUN/	86	Vcc	113	RID8
6	BEEP	33	RASH	60	PACKWRITE	87	KA16	114	Vcc
7	ROM	34	RASL	61	INTL	88	KA11	115	gnd
8	CVWS	35	KD14	62	INTH	89	KA10	116	LORA6
9	PACKREAD	36	KA21	63	40MHZ	90	KA8	117	LORA3
10	PTR3	37	KD12	64	Vcc	91	KA5	118	LORA0
11	PTR2	38	KD15	65	IOD01	92	KA2	119	CAS3
12	PTR1	39	KA22	66	IOD03	93	KD3	120	CAS2
13	8MHZCLK	40	KA23	67	IOD06	94	FC1	121	KD11
14	LBRW	41	KA18	68	GBA2	95	IPL0/	122	KA15
15	LSIO	42	KA14	69	GBA10	96	IORESET	123	gnd
16	IOD00	43	KA9	70	RID1	97	gnd	124	gnd
17	IOD02	44	KA7	71	RID4	98	IPL2/	125	KA12
18	IOD05	45	KA6	72	RID7	99	KD4	126	KA13
19	STDS	46	KA4	73	RID10	100	KD9	127	KD13
20	GBA11	47	KA3	74	RID12	101	DISACK	128	KD8
21	RID0	48	KA1	75	gnd	102	ALCH/	129	KD7
22	RID3	49	FC0	76	LORA9	103	COM_IC_SEL	130	KD5
23	RID6	50	FC2	77	LORA7	104	BAUDCLK	131	IPL1/
24	RID9	51	BERR/	78	LORA4	105	gnd	132	Vcc
25	RID11	52	KUDS/	79	LORA1	106	gnd		
26	RID13	53	gnd	80	CAS4	107	IOD04		
27	RID14	54	KRW/	81	CAS1	108	IOD07		

Figure 3-3. GLUE Gate Array (U518) pin configuration and signals.



Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	V_{DD}	25	V_{DD}	49	gnd	73	BBA6	97	V_{DD}
2	N/C	26	R0	50	BD13	74	ABR9	98	BD7
3	BD15	27	BBA2	51	BD12	75	BBA9	99	DIRX3
4	HSX1	28	ABR4	52	HSX4	76	BBA10	100	VRS
5	HSX2	29	BBA7	53	HSX5	77	R7	101	EE4
6	HSX3	30	ABR12	54	BBA13	78	gnd	102	ABR7
7	ABR8	31	BBA3	55	TRIG100	79	N/C	103	WEL
8	VE1	32	BBA1	56	BD1	80	R15	104	ABR5
9	SRT	33	IORESET/	57	HSI	81	BBA14	105	gnd
10	BD0	34	VE2	58	gnd	82	S_CK1	106	BBA12
11	BD3	35	R6	59	SDI	83	R8	107	BBA8
12	R5	36	R13	60	BD5	84	R11	108	ABR11
13	gnd	37	gnd	61	BD6	85	SDX3	109	ABR10
14	R1	38	R2	62	DIRX2	86	SDX4	110	BBA11
15	BD4	39	R9	63	ABR6	87	BD14	111	VE3
16	DIRX1	40	R12	64	EE1	88	R4	112	N/C
17	DIRI	41	TLGA_SEL/	65	EE2	89	gnd	113	V_{DD}
18	ETRIG	42	R14	66	ABR0	90	BD9	114	R3
19	RUN_STOP	43	BBRW	67	BBA4	91	BUDS/	115	EVT
20	EE3	44	SDX1	68	N/C	92	HSX6	116	OEL
21	COMINT	45	SDX2	69	gnd	93	VE4	117	S_CK2
22	BTC	46	R10	70	ABR3	94	BDTACK	118	SDX6
23	ATC	47	BD8	71	BBA5	95	BD2	119	BD11
24	ABR1	48	BLDS/	72	ABR2	96	SDX5	120	BD10

Figure 3-4. TekLink Gate Array (U720) pin configuration and signals.



Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	M11	28	BBA6	55	M15	82	BDTACK	109	TVE
2	M12	29	BBA9	56	N/C	83	INTACK	110	N/C
3	M14	30	BBA11	57	N/C	84	M1	111	IORESET/
4	N/C	31	BBA12	58	N/C	85	M5	112	N/C
5	N/C	32	BBA13	59	KEL/	86	V_{CC}	113	TCE
6	N/C	33	BBRW	60	HSYNC	87	M7	114	VCL
7	N/C	34	BUDS/	61	EN	88	RA7	115	gnd
8	KEH	35	VIDEO_INT	62	PIX3	89	RA5	116	BBA4
9	VSYNC	36	40MHZ	63	PIX1	90	RA3	117	IORESET/
10	SCLK	37	M0	64	V_{CC}	91	RA1	118	N/C
11	PIX2	38	M2	65	N/C	92	RA10	119	N/C
12	PIX0	39	M4	66	BD1	93	RA9	120	N/C
13	N/C	40	M3	67	BD3	94	RA13	121	N/C
14	BBA14	41	M6	68	BD5	95	RA14	122	N/C
15	BBA15	42	RA12	69	BD7	96	M9	123	gnd
16	BBA16	43	RA6	70	BD9	97	gnd	124	gnd
17	BD0	44	RA4	71	BD11	98	TTC	125	N/C
18	BD2	45	RA2	72	BD13	99	N/C	126	N/C
19	BD4	46	RA0	73	BD15	100	TCC	127	N/C
20	BD6	47	RA15	74	BBA2	101	N/C	128	N/C
21	BD8	48	RA11	75	gnd	102	TEE	129	N/C
22	BD10	49	RA8	76	BBA7	103	N/C	130	N/C
23	BD12	50	MRW	77	N/C	104	TST1	131	N/C
24	BD14	51	M8	78	BBA8	105	gnd	132	V_{CC}
25	BBA1	52	M10	79	BBA10	106	gnd		
26	BBA3	53	gnd	80	VGA_SEL/	107	TST0		
27	BBA5	54	M13	81	BLDS/	108	N/C		

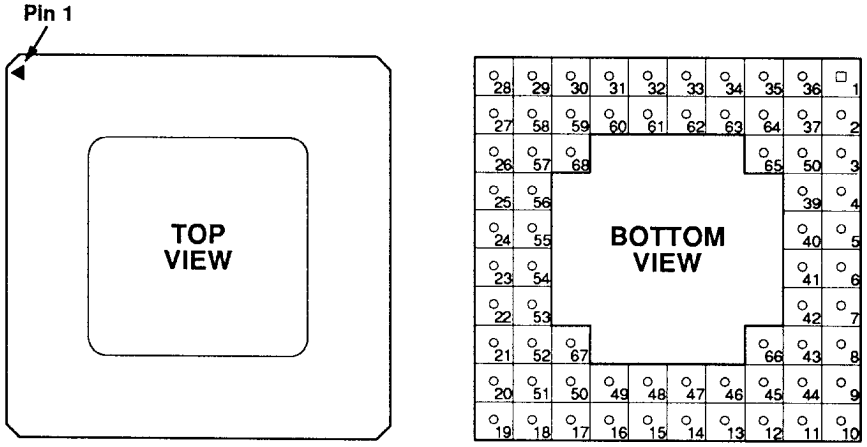
Figure 3-5. Video Gate Array (U745) pin configuration and signals.

68010 PROCESSOR PIN CONFIGURATION AND SIGNALS

Figure 3-6 shows the pin configuration and signal assignments for the Motorola 68010 microprocessor from the back (non-component) side of the MPU board.

NOTE

Most of the 68010 signals can be accessed from the component side of the board at the GLUE Gate array. Refer to Figure 3-3 for signal locations on the GLUE gate array.



Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N/C	18	KA9	35	KD1	52	KA12
2	DTACK/	19	N/C	36	KAS/	53	KA15
3	BGACK	20	KA14	37	KLDS/	54	KA18
4	BR	21	KA16	38	BG	55	V_{CC}
5	10MHZ	22	KA17	39	V_{CC}	56	gnd
6	HALT/	23	KA19	40	gnd	57	KA23
7	VMA	24	KA20	41	CPU_RESET/	58	KD14
8	1MHZ	25	KA21	42	VPA	59	KD11
9	BERR/	26	KA22	43	IPL2/	60	KD9
10	N/C	27	KD15	44	IPL0/	61	KD6
11	FC2	28	KD12	45	FC1	62	KD3
12	FC0	29	KD10	46	N/C	63	KD0
13	KA1	30	KD8	47	KA2	64	KUDS/
14	KA3	31	KD7	48	KA5	65	KRW
15	KA4	32	KD5	49	KA8	66	IPL1
16	KA6	33	KD4	50	KA10	67	KA13
17	KA7	34	KD2	51	KA11	68	KD13

Figure 3-6. 68010 Processor pin configuration and signals.

TEST POINTS AND TEST CONNECTORS

The MPU board has several connectors that can be used for test purposes. These connectors are typically used for field service and factory repair or troubleshooting. Figure 3-1 shows the location of the following test points and connectors:

J105–REMOTE RESET. A momentary short between pins 1 and 2 (via a remote switch closure) causes a reset of the MPU system (power does not cycle).

J285–SPEAKER OUTPUT/CONTROL. Pin 1 is for an external amplifier and speaker connection. Grounding pin 3 shuts off the board-mounted speaker circuit. Pin 2 is ground.

J390–DIAG TEST TRIGGER. Provides a high-active TTL trigger signal each time a system diagnostic test (excluding Kernel Diagnostic tests) is initiated. Can be used to trigger test equipment.

J460–CAL FREQ. Test point used when verifying or adjusting Calendar Chip Oscillator.

J505–REMOTE OFF. Pin 1 can be used as either a test point to monitor pin 5 of the power control integrated circuit (U205), or it can be grounded to provide a remote power-off cycle. Pin 2 is ground.

J560–NMI SWITCH. Used for low-level diagnostics of compute kernel circuitry. A momentary short between pins 1 and 2 (ground) starts the Kernel Test Monitor software routine. A terminal can access the Kernel Test Monitor via one of the RS-232-C ports. (If an RS-232-C COMM Pack is installed, the Kernel Test Monitor uses the COMM Pack port; otherwise, it uses the RS-232-C host port.)

Section 4
THEORY OF OPERATION

INTRODUCTION

This section describes the electrical operation of the MPU boards. The discussion goes from the general to the specific. Differences between the boards are provided, as needed, throughout the following descriptions. Functionally, these boards are the same. The differences are related primarily to the Display and TekLink connectors. These descriptions, together with the troubleshooting and diagnostic sections enable a technician to isolate a problem to the faulty component.

NOTE

Refer to Section 3: Connectors and Cabling *for a detailed description of the Display and TekLink connectors.* Section 11: Diagrams *contains separate component location drawings for different versions of the MPU board. The MPU circuit schematics also show the electrical differences.*

This section serves two primary purposes:

1. Provides an excellent source of information by which to teach product theory to service technicians.
2. Serves as an information source when performing component-level repair.

This section contains the following:

- **Logic Conventions** describe how logic functions are performed and represented in this manual.
- **MPU System Overview** describes the major electrical modules that can be associated with an MPU board.
- **MPU Detailed Descriptions** provide detailed explanations of MPU circuit theory.

LOGIC CONVENTIONS

Digital logic techniques are used to perform logic functions within the MPU circuits. The functions and operations of the logic circuits are represented by standard logic symbols and terms. Logic functions are described using the positive logic convention: the more positive of two levels is the true, or 1 state; the more negative level is the false, or 0 state.

In Logic descriptions, the more positive of the two logic voltages is referred to as high; the more negative state is referred to as low.

NOTE

The specific voltages that constitute a high or low state vary between different electronic devices (ECL, CMOS, and TTL logic).

Active-low signals are indicated by either an L, a slash (/) or a tilde (~) following the signal name or by an underscore (_) preceding the signal name. Signal names without indicators are considered to be either active-high or to have both active-high and active-low states. Some active-high signals are indicated by an H following the signal name.

MPU SYSTEM OVERVIEW

Figure 4-1 shows the major functional circuits on the MPU board. The information that follows describes the basic operation of each functional circuit. (*Section 1: General Information* provides an overview of the functional modules associated with an MPU board. Specific information regarding functional modules is provided in separate service manuals.)

General

The MPU is a single-board host computer that provides central control and memory for a mainframe system. It is based on a 68010 microprocessor, 2 Mbyte or 4 Mbyte of RAM, and 32 Kbyte of boot ROM. Much of the MPU electronics is contained in three gate arrays that perform:

- MPU support functions—GLUE gate array
- Display control and interface functions—Video gate array
- Acquisition module communication support functions—TekLink gate array

The MPU provides a standard RS-232-C port for keyboard (or console) and host communications. It also provides a generic Tektronix 1200-Series COMM Pack port for RS-232-C, GPIB, and printer interfacing. A 640 X 400, non-interlaced display output from the video gate array provides connection for an external monitor. A 3.5 inch floppy disk drive functions as the standard system disk. A hard disk drive is connected to the MPU board for mass storage. The hard disk drive is optional for the 3001 mainframes.

System software is based on a real-time operating system (pSOS). Its MS-DOS ® compatible file system has been specially modified for the instrumentation environment. A full set of general purpose utilities supports a menu-based user interface. Basic external communications software provides system control and transfer of binary information.

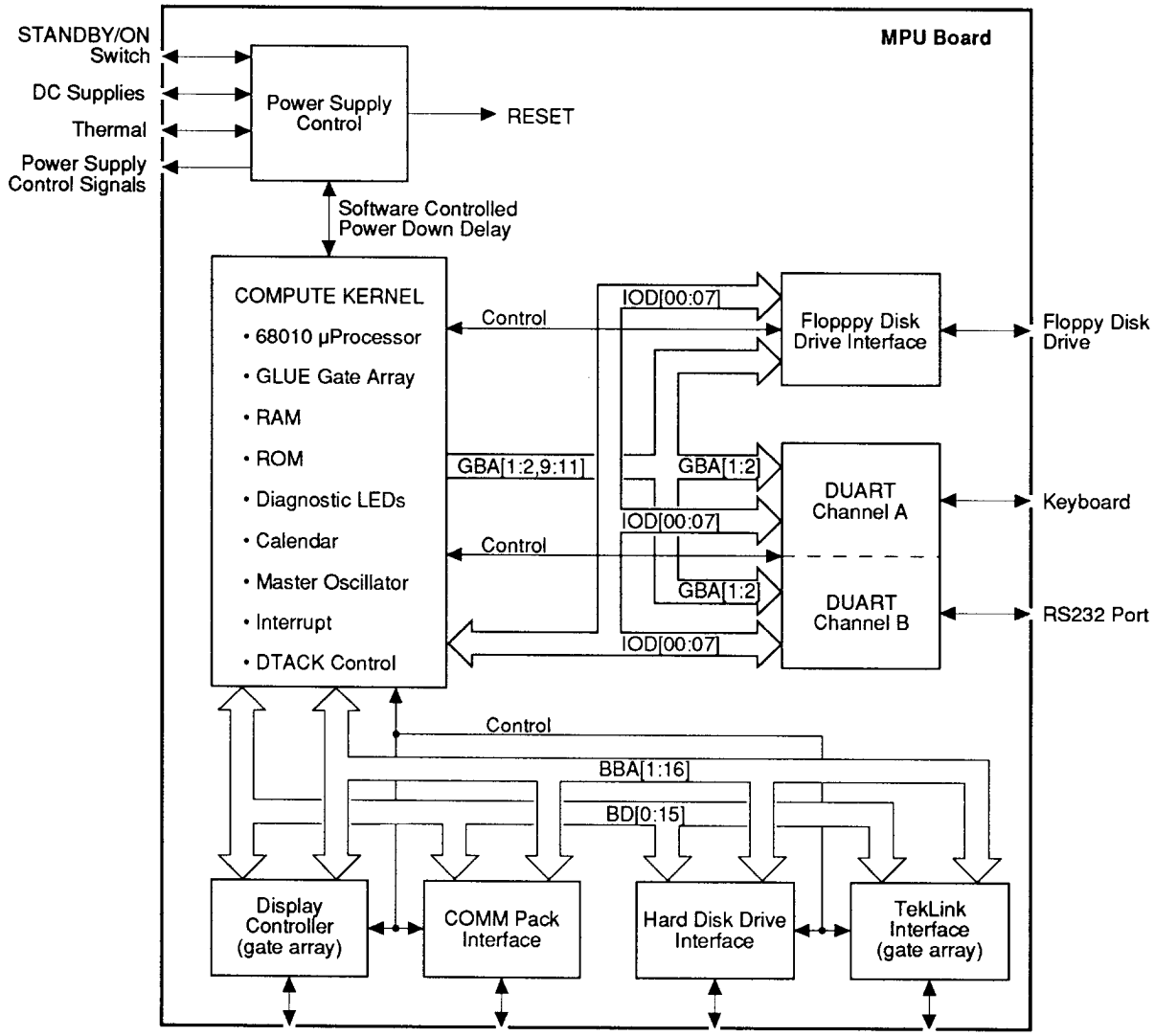


Figure 4-1. MPU board block diagram.

Compute Kernel

The Compute Kernel consists of circuits critical to the boot process. It includes the 68010 processor, RAM, ROM, GLUE gate array, interrupt control, DTACK control, clock (calendar), and other components.

Floppy Disk Interface

The primary interface component of the floppy disk interface is a Western Digital 1772 Flexible Disk Controller/Formatter IC. All floppy disk data communication to and from the MPU circuitry is via the IOD[00:07] bi-directional data bus, and associated control lines. Addressing is via selected bits of the GLUE address bus.

A 720 Kbyte (formatted) floppy disk drive provides storage of the operating system, diagnostics, applications software, and acquisition data files. The drive uses 3.5 inch, hard-shell floppy disks.

Hard Disk Interface

Data transfer between the MPU board and the hard disk drive is managed by a Hard Disk Controller board for the ST506/412-interface hard disk drives and by an IDE Interface board for the IDE-interface hard disk drives. The MPU board contains tri-state buffer/drivers for interfacing and isolating its address and data buses from the Hard Disk Controller or the IDE Interface board. Refer to the applicable mainframe service manual for a description of the Hard Disk Controller or the IDE Interface board circuitry.

Keyboard/Host DUART

The keyboard (or console) and RS-232-C host use a Signetics 2681 DUART (and other GLUE logic) to interface with the MPU. The 2681 is a two-channel IC; channel A is the keyboard interface and channel B is the host interface. Both channels are full-duplex asynchronous. The DUART contains a 7-line input port and an 8-bit data output port. The IC accepts a baud clock from the GLUE gate array. The IC provides interrupt control and operational control for the read, write, and address decoding functions. Address decoding (inside the 2681) is done using the GLUE bus address bits GBA[1:2] and the buffered address bits 3 and 4.

COMM Pack Interface

The COMM Pack interface circuits interface between the MPU address and data buses and Tektronix 1200-series communication packs.

Communication packs provide a customized communications link between the MPU and an external device or controller. COMM Packs are available for RS-232-C, GPIB, and 8-bit parallel printer protocols.

COMM Packs plug into a connector mounted directly on the MPU board. The MPU manages all COMM Pack communications.

Display Controller

The MPU board, via the Video gate array, provides a 640 X 400 pixel, non-interlaced display output to drive a display monitor. It can drive a color CRT, a monochrome CRT, or a flat-panel display.

Characters are displayed using a programmable character set (8 X 10 cell with full descenders and underlining). Normal and inverse video is provided. Color attributes can be specified.

The Video gate array supports bit-mapped graphics. Character and graphics data can be displayed in either one or two windows; contents of a window are smooth-scrolled, both vertically and horizontally, at a rate of 50 lines per second.

TekLink Interface

Acquisition modules interface to the MPU by using TekLink, a high-speed serial data interface.

TekLink consists of a 26-pin bus used for serial data transfer between the MPU board and acquisition modules, and for synchronizing events between acquisition modules. TekLink identifies acquisition modules as being internal or external to a mainframe system. TekLink protocol facilitates system configuration, acquisition module setup, run time control, and data read-back for any connected internal and external modules.

Service information for each Tektronix acquisition module is provided in acquisition module service manuals.

Power Supply Control

The MPU receives +5 VDC, +12 VDC, and –12 VDC from the mainframe power supply.

The MPU board has circuitry that functions as an electronic power switch to control the on/off state of the power supply. When the STANDBY/ON switch is pressed ON, this circuitry causes the power supply to start delivering power to the MPU board and any connected acquisition modules within the mainframe.

This circuitry also controls the power-off process, providing power-off delay (which can be software-controlled to extend the amount of delay). Power will also be shut down in the event of a power supply failure or an excess temperature condition on an acquisition module.

MPU BOARD DETAILED DESCRIPTIONS

Introduction

The rest of this section provides detailed functional descriptions of the MPU board electronic components. Information is presented in the following order:

- How to Use the MPU Circuit Descriptions
- Using the Detailed MPU Board Block Diagram and Schematics
- 68010 Processor
- MPU Bus Architecture
- Power Control Descriptions
- Compute Kernel Description
- Floppy Disk Interface Description
- Hard Disk Interface Description
- Video Controller Description
- RS-232
- RS-232-C (Keyboard and Host) Interface Description
- Communications Pack Interface Description
- TekLink Interface Description

How to Use the MPU Circuit Descriptions

These descriptions are presented in a manner that supports efficient troubleshooting of MPU hardware failures. Information is grouped in much the same manner as the System Diagnostics Software for the MPU board. For example:

Assume that you have a problem with the video controller circuit. Your should first exercise the series of video diagnostic tests (both the *video* and *display* area tests). You would then note the pass/fail status of each test routine and the index information for any failed tests. At this point you should read the detailed troubleshooting information for the index numbers provided as part of the diagnostic test description. If you need additional troubleshooting information regarding the failed circuit, you can then reference the video controller circuit descriptions provided in this section.

Using the Detailed MPU Board Block Diagram and Schematics

A detailed block diagram of the MPU board circuits is located in the *Section 11: Diagrams*. That diagram shows the signal connections between each functional block of circuitry. Schematic reference numbers are located within each circuit block. Those numbers indicate the schematic diagrams where the detailed circuitry associated with a particular function is located. Refer to the block diagram and/or schematics as you read the following functional circuit descriptions.

68010 Processor

The following description provides a functional overview of each 68010 signal, describing how the signal is used by the MPU electronics. (Refer to a 68000 data sheet for details regarding 68010 microprocessor operation.)

Figure 4-2 shows the signals associated with the 68010 microprocessor. Signals are categorized as:

- Bus address and data lines
- Bus control signals
- System control input signals

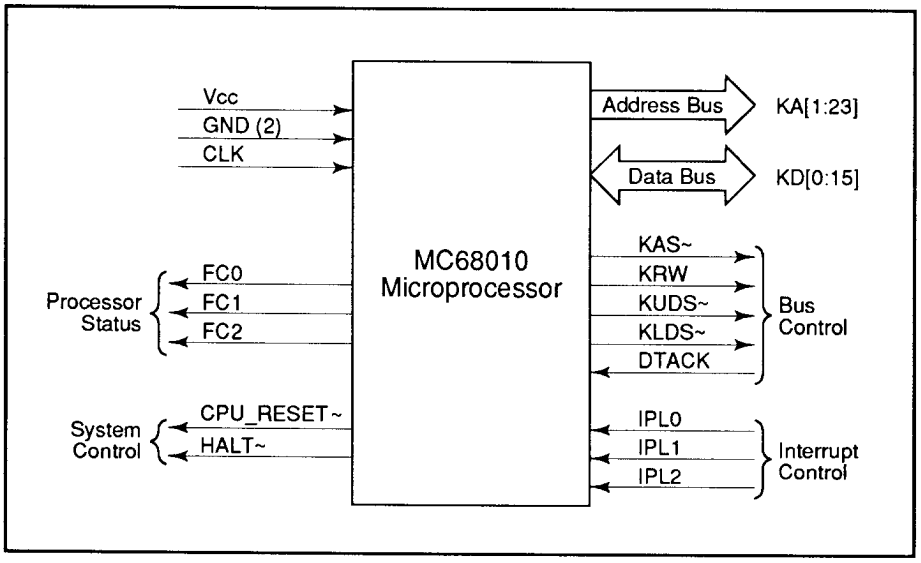


Figure 4-2. 68010 input and output signals.

The following paragraphs provide a brief description of each signal. Refer back to Figure 3-6 for an illustration that shows the 68010 pin signal assignments.

NOTE

Microprocessor data and address lines, and some control signals, are identified by the letter "K." The letter "K" differentiates these signals from their buffered counterparts. These "K" lines are critical to CPU operation and must be functional for any diagnostic software to execute.

Bus Address and Data Lines

Data and address lines consist of the following:

KA[1:23]. A 23-bit, one-direction three-state address bus that carries the device address bits for bus operations, except for CPU space cycles.

KD[00:15]. This 16-bit, bi-directional, three-state data bus is the general purpose data path. It can transmit and receive data in either word format (8-bit) or byte format (16-bit) .

Bus Control Signals

Data is transferred asynchronously using the following control signals:

KAS/. This signal indicates that there is a valid address on the address bus.

KRW. This signal defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the data strobes KUDS/ and KLDS/.

KUDS/. This signal controls the flow of data on the data bus as shown in Table 4-1. When KRW is high, the microprocessor reads from the data bus, as indicated.

KLDS/. This signal controls the flow of data on the data bus as shown in Table 4-1. When KRW is low, the microprocessor writes to the data bus, as indicated.

Table 4-1
Data Strobe Control of Data Bus

KUDS/	KLDS/	KRW	D[8:15]	D[0;7]
1	1	X	No valid data	No valid data
0	0	1	Valid data bits 8–15	Valid data bits 0–7
1	0	1	No valid data	Valid data bits 0–7
0	1	1	Valid data bits 8–15	No valid data
0	0	0	Valid data bits 8–15	Valid data bits 0–7
1	0	0	Valid data bits 0–7	Valid data bits 0–7
1	1	0	Valid data bits 8–15	Valid data bits 8–15

DTACK (data transfer acknowledge). This input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched one clock cycle later and the bus cycle terminated. When DTACK is recognized during a write cycle, the bus cycle is terminated.

IPL0/, IPL1/, and IPL2/ (interrupt control). These input pins indicate the encoded priority level of the device requesting an interrupt. Level 7 is the highest priority while level 0 indicates that no interrupts are requested. Level 7 cannot be masked. The least significant bit is IPL0/ and the most significant bit is IPL2/. These lines must remain stable until the processor signals interrupt acknowledge [FC0:2] are all high and [A16:19] are all high to insure that the interrupt is recognized.

System Control Inputs

System control signals either reset or halt the processor and indicate to the microprocessor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BERR (bus error). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

- non-responding devices
- interrupt-vector number-acquisition failure

RESET/ (reset). This bi-directional signal line resets (starts a system initialization sequence) the microprocessor in response to an external reset signal. An internally generated reset (result of a reset instruction) causes all external devices to be reset. The internal state of the microprocessor is not affected. A total system reset (microprocessor and external devices) results when external HALT/ and RESET/ signals are applied at the same time.

HALT/ (halt). When this bi-directional line is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are set to their high-impedance state (refer to Table 4-2).

When the microprocessor has stopped executing instructions due to a double bus fault condition, the HALT/ line is driven by the microprocessor to indicate to external devices that the microprocessor has stopped.

FC0, FC1, and FC2 (processor status). These function code outputs indicate the state (user or supervisor) and the address space currently being accessed, as shown in Table 4-2. The information indicated by the function code outputs is valid whenever address strobe KAS/ is active.

Table 4-2
Address Space Selection

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

CLK (clock). A 10 MHz clock is input to the processor from the GLUE gate array. CLK is a TTL-compatible signal that is internally buffered for the development of the internal clocks needed by the microprocessor.

MPU Bus Architecture and Block Diagram

Figure 4-3 shows the bus architecture of the MPU board. The 68010 transfers data using separate parallel buses for address and data, KA[01:23] and KD[00:15], respectively. As shown, the address and data buses connect directly to EPROM, LED registers, GLUE gate array, and kernel address and data buffers. The kernel address and data buses are indirectly connected to the COMM Pack, Hard Disk Controller board, Video gate array, and TekLink gate array via the kernel address and data buffers. Buffered address bits 3 and 4 also connect to the real-time clock and to the DUART circuitry.

The GLUE gate array uses three distinct address and data buses for data transfer between connected circuitry:

- KA[01:16] and KD[00:15] for data transfer to/from the 68010 and to/from the COMM Pack, hard disk, and other circuits, via kernel address and kernel data buffers.
- LORA[0:9] and RID[0:15] for data transfer to and from the system DRAM.
- GBA[1:2] and IOD[00:07] for data transfer to and from the real-time clock, DUART (keyboard and Host), and flexible disk.

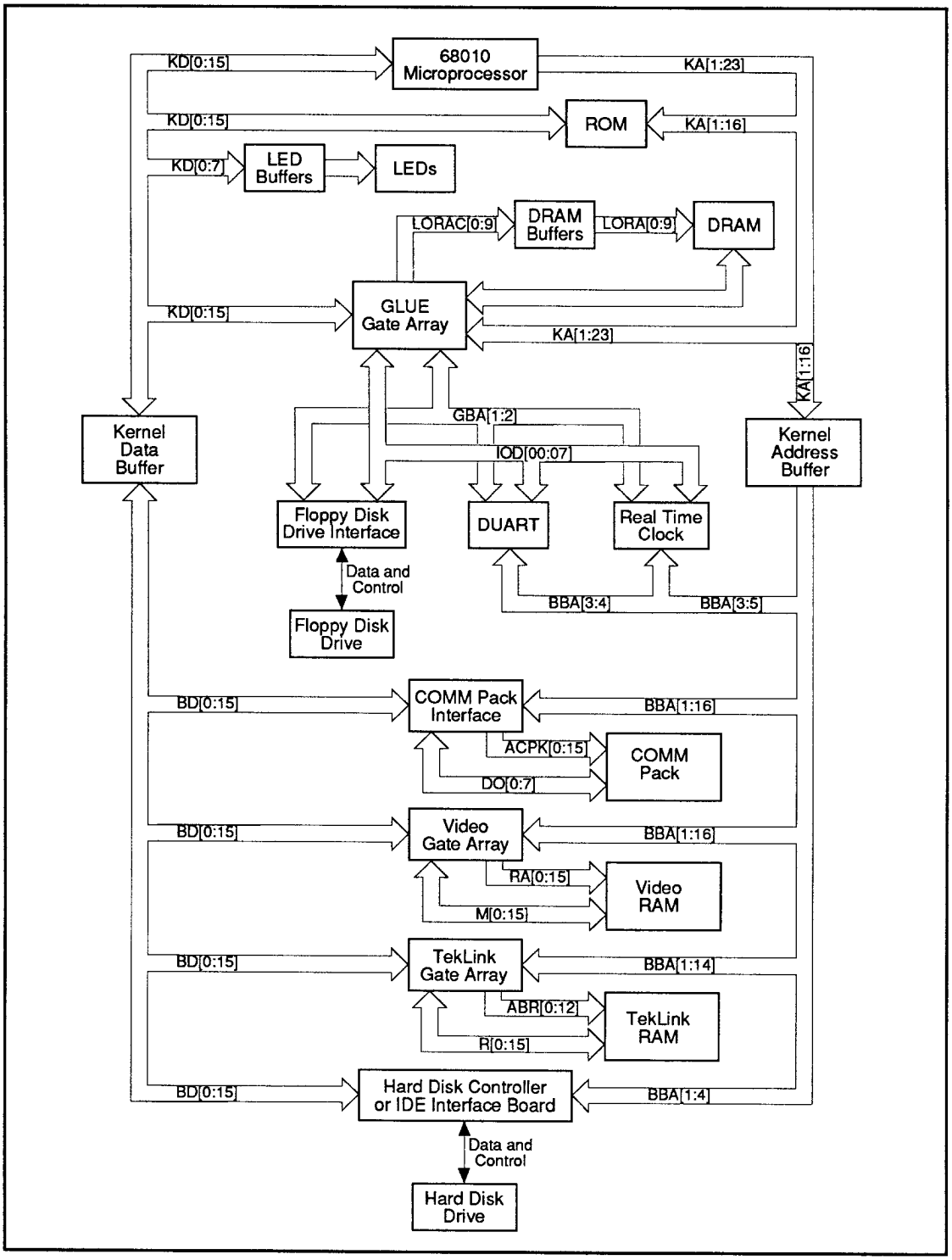


Figure 4-3. MPU bus architecture diagram.

Power Control Description

Introduction

The MPU board has circuitry that functions as an electronic switch to control the on/off state of the power supply. When the front-panel STANDBY/ON switch is pressed ON, this circuitry causes the power supply to "turn on." As the power supply turns on, the +5 V supply line is sensed, keeping MPU reset signals active until +5 V reaches its nominal voltage level. When +5 V reaches the nominal level, the MPU logic is set to a known condition. Then the power-on circuits deactivate the reset line, and the compute kernel initiates the power-on boot sequence.

Details of power-on and power-off operations are as follows. Refer to MPU Board Schematic 12 and the block diagram in *Section 11: Diagrams* when reading this.

Power-On

When the Mainframe STANDBY?ON switch is pressed ON, pin 6 of U205 is grounded, causing U205 to ground pin 10, the REMOTE_ON_OFF signal. A ground potential on REMOTE_ON_OFF causes the power supply to turn on. As the +5 V supply comes up, a silicon-controlled rectifier (within U205) turns on, clamping pin 10 of U205 to ground, thus maintaining the power-on condition.

During power-on, the +5 V supply is sensed by U211, which keeps its RESET and RESET/ outputs active (high and low, respectively) as long as the +5 V supply has not reached its nominal voltage. The RESET signals activate the processor reset lines: CPU_RESET/, RESET_LED, IO_RESET, and IORESET/. These lines effectively hold the 68010 processor and other MPU circuits in a reset condition.

When the +5 V supply has reached its nominal voltage, U211 initiates an internal time delay, holding its RESET lines active. This delay ensures that the MPU has reset. This delay is set by C210. Once C210 is charged, U211 returns the RESET and RESET/ lines to their inactive states.

Power-Off

Power-Off is controlled as follows:

1. User switches the Mainframe STANDBY/ON switch from ON to STANDBY.
2. User applies a remote power-off signal, or an acquisition module grounds the THERM signal line.
3. Software uses the software-controlled power-off delay feature.

Using STANDBY/ON Switch. When the STANDBY/ON switch is set to STANDBY, KILL_POWER is grounded via pin 1 of J160. This causes an interrupt into the microprocessor, warning the system that a power shutdown is pending. The power supply "turns off" as follows:

When pin 1 of J160 is grounded, Q402 (Q511)* turns off. C500 begins to charge. Transistors Q402 (Q511), Q403 (Q510), and Q404 (Q505), and capacitor C500 then function as a shutdown delay circuit. (During the power-on process, KILL_POWER is at +5 V, causing Q 402 (Q511) to turn on, discharging C500. This keeps the Darlington pair, Q403 and Q404 (Q510 and Q505), off, maintaining a high at pin 12 of U205.) After ≈2 seconds, C500 is fully charged to ≈1.2 V, turning the Darlington pair on. (The power-off delay provided by C500 allows the MPU system software time to save any applications that may be running before power is shutdown. Refer to *Software Controlled Power-Off Delay* later is this section for additional information.)

When C500 is fully charged, causing the Darlington pair to turn on, ground potential is placed at pins 12 and 5 of U205. The high REMOTE_ON_OFF signal shuts down the power supply.

Remote Shut-down. The power supply can shut down with an active low THERM signal or a ground at J505, pin 1 (J505 is for connecting a remote on/off test switch).

Thermal Signal Shut-down. Any acquisition module connected to the MPU board via the TekLink interface provides thermal protection. If an acquisition module experiences a thermal condition, it pulls the THERM signal line to ground potential. The THERM line can be grounded by internal acquisition modules (via J810 pin 10) or external acquisition modules (via J910 pin 10). A high temperature condition places ground potential at pins 5 and 12 of U205, thus shutting down the power supply via a high-level REMOTE_ON_OFF signal.

Remote ON/OFF Test Switch. You can connect a remote switch to J505 on the MPU board. A ground at pin 1 of J505 causes J204 to set REMOTE_ON_OFF high, thus shutting down the power supply.

CAUTION

A power-off condition caused by a THERM signal or a ground at J505 pin 1 bypasses the delay feature. The HALT/ signal is activated to stop the microprocessor after the current bus cycle is completed. Consequently, set-ups and other important applications data could be lost.

Software Controlled Power-Off Delay. In some circumstances, an application may require more than the two-second power-off delay set by C500. The power-off cycle can be delayed by software control in the following manner:

* *Circuit numbers in parentheses were used with the first version of the MPU board.*

A grounded KILL_POWER line (caused by applying ground potential at J160, pin 1) causes an interrupt, signaling the processor that a power-off cycle is in progress. The processor checks the interrupt source, determines that a power-off cycle is in process, then determines if power-off sequence should be delayed until current operations are completed (to save set-ups, etc). To delay the power-off cycle, the kernel circuitry addresses and strobes U438, using KA23. The resultant strobe action at the base of Q 402 (Q510) prevents C500 from charging. When the microprocessor is ready for shutdown, it stops strobing U438, allowing C500 to charge and the power supply shuts down as previously described.

Compute Kernel Circuit Descriptions

Introduction

The compute kernel consists of circuits critical to the boot process. The following provides a general description of the boot process and power-on diagnostics. This is followed by detailed descriptions of each compute kernel circuit.

Boot Process–General Description

Refer to the MPU Board Detailed Block diagram in the *Section 11: Diagrams* when reading the following.

When the MPU is reset following a power-on condition, the 68010 causes the GLUE gate array to enable the ROM. The 68010 addresses specific ROM locations for an initial command sequence. The boot ROM contains instructions that direct the processor to run power-on diagnostics. Following the successful completion of ROM-based power-on diagnostics, boot code loads the operating system from system disk and prepares the system for normal operation.

If an error is detected when performing an automatic power-on diagnostic test, the boot process is halted and the diagnostics attempts to display an error message in two ways:

1. By writing to the display unit, and
2. By displaying an error code on a set of diagnostic LEDs (these LEDs are mounted on the MPU board).

The error message indicates the point in the power-on process where the failure occurred. The test that fails continually loops at the point of failure, enabling the technician "probe and test" to locate the defective part.

NOTE

Under certain circumstances, the message sent to the display monitor will not appear. For example, the message doesn't appear if the display monitor fails or if activating the display monitor could crash the system.

Refer to *Section 8: Troubleshooting* and *Section 9: System Diagnostic Software* for additional details on power-on sequencing and diagnostic tests, respectively.

Circuit Description

The compute kernel consists of the following circuits.

- Master clock
- 68010 processor
- GLUE gate array
- Diagnostic LEDS
- Read only memory (EPROM)
- Random access memory (DRAM)
- 68010 data and address bus buffers
- Bus control signal buffers
- Interrupt multiplexer
- DTACK control
- Calendar (real-time clock)

Each circuit is described in detail in the following material. Refer to the MPU Board Detailed Block Diagram in *Section 11: Diagrams* when reading the following descriptions.

Master Clock. YG610 (Schematic 5) provides a 40 MHz clock signal to the GLUE gate array. The GLUE gate array divides the clock into several clock frequencies as follows:

- 10 MHz. Used as master clock for 68010 microprocessor.
- 8 MHz. Used as master clock for flexible disk controller/formatter.
- BAUD CLK. Used as baud-rate clock for keyboard and host communications.

68010 Processor. The basic functions of the 68010 have been described earlier in this section. Refer to *68010 Signal Descriptions* for detailed description of signals. Refer to the Motorola 68000 data book for additional details regarding 68010 operations.

GLUE Gate Array. The GLUE gate array, U518, supports the 68010 microprocessor as it interacts with the rest of the system. Primarily, it provides the following:

- Microprocessor support circuitry such as (1) address decoding and interrupt vector generation, (2) bus error (BERR) detection and memory management, and (3) system clocking
- DRAM control
- Address decoding for the Hard Disk Controller board.
- COMM Pack port support logic
- Audio tone generator
- DMA between DRAM and floppy-disk drive

GLUE Normal Use Registers. Table 4-3 shows a listing of the GLUE normal use registers and their addresses. The following text explains them in greater detail.

Table 4-3
Glue Gate Array Normal Use Register Addresses

Register Function/Name	Address	Access	Read/Write
DMA command latch	85F170	Supervisor	Read/Write
DMA target address counter (high byte)	85F172	Supervisor	Read/Write
DMA target address counter (low word)	85F174	Supervisor	Read/Write
DMA limit counter	85F176	Supervisor	Read/Write
DMA temporary data storage register	85F178	Supervisor	Read/Write
Beeper control latch	85F17A	Supervisor	Read/Write
Interrupt inhibit mask latch	85F17E	Supervisor	Read/Write
Interrupt request status register	85F17C	Supervisor	Read Only

The following is a brief description of each normal use register.

DMA Command Latch. This 4-bit read/write register uses bits 0 and 1 for DMA control. Bits 2 and 3 are used to protect the "zero-page" of RAM from writes by the user space code. Bit functions are as follows:

Table 4-4
Glue Command Latch Bit Functions

Bit Number				Condition
3	2	1	0	
X	X	X	0	Move data to floppy disk
X	X	X	1	Move data from floppy disk
X	X	0	X	Disable DMA operations
X	X	1	X	Enable DMA operations
0	0	X	X	64K protected RAM
0	1	X	X	32K protected RAM
1	0	X	X	128K protected RAM
1	1	X	X	256K protected RAM

DMA Target Address Counter. This is a 24-bit counter/register occupying address locations 85F172-85F174. When a DMA operation is initiated, this register is loaded with the RAM starting address from which data will be obtained to write to the floppy disk. At the beginning of a floppy read operation, this register will contain N-2, where N is the RAM address to where data from the floppy will be first written.

DMA Limit Counter. When a DMA operation is initiated, this 16-bit register is loaded with the value 0XFFFF-N where N is the number of bytes to be moved to or from the floppy disk. DMA will halt when the value of 0XFFFF is in this register. A power failure interrupt is a special situation that will halt DMA when bits 0-8 are all ones. This stops DMA at the completion of a disk sector read/write operation.

DMA Temporary Data Storage Register. This 16-bit register can be thought of as an interface between RAM and the floppy disk controller. RAM reads/writes 16 bits at a time whereas the floppy controller reads/writes 8 bits (one byte) at a time. When data is transferred from RAM to floppy disk, the entire 16-bit word is first loaded into this register, then it is loaded one byte at a time into the floppy controller. When a disk is read, the floppy controller loads one byte at a time into this register. After two bytes are loaded, the register writes the contents into RAM.

Beeper Control Latch. This 16-bit register controls three functions: beeper period value (frequency), beeper volume, and the delayed-Off feature.

- Beeper period value (frequency). Bits 0-11 control beeper period value. The actual period = period value times 2.7125 µs. Frequency = 1/period; therefore, the inverse of these bits controls the frequency.
- Delayed-Off feature. Bit 12 controls the On/Delayed-Off feature. Delayed-Off provides a 0.7 second delay when bit 12 is high.
- Beeper volume. Volume is controlled by bits 13-15. See Table 4-5 for volume values.

Table 4-5
Programmable Volume Values

Volume Bit			
13	14	15	Volume/Duty Cycle
0	0	0	100%
0	0	1	50%
1	0	1	25%
0	1	1	12.5%
1	1	1	6.25%
1	X	0	0%

A volume/duty cycle of 25% is considered normal volume. A 100% duty cycle should be loud enough to annoy anyone within 15 feet of the instrument.

NOTE

When the MPU powers on, the volume/duty cycle is set at 0%.

Interrupt Inhibit Mask Latch. This 16-bit register permits masking of any interrupt source with one mask bit per source. Table 4-6 lists the bit designations.

Table 4-6
Interrupt Inhibit Bit Designations

Bit	Interrupt Source
0	Keyboard transmit (lowest priority)
1	Keyboard receive
2	Low battery
3	Hard disk
4	2681 IRQ
5	1240/1260 COMM Pack
6	RS232 transmit
7	RS232 receive
8	Display
9	TekLink
10	Floppy IRQ
11	Clock tick
12	Kill power (STANDBY/ON switch)
13	Floppy DRQ
14	NMI button
15	Power failure (highest priority)

Interrupt Request Status Register. This 16-bit register simply indicates the status of the previously mentioned interrupts. It is read-access only. The bit designations are identical to those of the interrupt inhibit mask latch (see Table 4-6). A bit value of 1 indicates a pending interrupt while a bit value of 0 is an inactive interrupt.

GLUE I/O Address Windows. Table 4-7 defines the GLUE I/O address window assignment and is followed by a detailed description of each listing.

Table 4-7
Glue I/O Address Window Assignments

FC(0,1,2)	Address Range	Device Function
1,2,5,6	000000–7FFFFF	DRAM access window
1,2,5,6	000000–01FFFF	Phantom ROM window
1,2,5,6	800000–81FFFF	Normal ROM access window
5	840001–84FFFF	Byte II/O access window
5	850000–85EFFF	Winchester disk controller
1,5	860000–87FFFF	Video display controller
5	F00000–F0FFFF	TekLink Interface
5	FE0001–FFFFFF	1240 COMM Pack
5	FE0000–FFFFFF	1260 COMM Pack
3	020000–3FFFFF	Diagnostic LEDs
3	D1E0FF	Power keep alive

DRAM Access Window. This is user access RAM. It is storage for user programs and data.

Phantom ROM Window. ROM code appears here immediately after the mainframe is powered on but will be replaced by DRAM access after any write to address 800000-81FFFF.

Normal ROM Access Window. This same ROM code appears as a phantom ROM window immediately after a power reset. This window can be accessed as program or data by user or supervisor.

Byte I/O Access Window. Standard LSI I/O devices like the floppy-disk controller appear in this memory space. These are only accessible as supervisor data (FC[0:2]=5) on odd addresses (bits 0-7).

Winchester Disk Controller. This address space is used for the Winchester disk controller and can only be reached as supervisor data (FC[0:2]=5).

Video Display Controller. The display can be accessed by both the user and the supervisor. Access is data and is not available as program space.

TekLink Interface. TekLink interface addresses can only be reached as supervisor data (FC[0:2]=5).

1240 COMM Pack. This address range can only be reached as supervisor data (FC[0:2]=5). COMM Packs should be addressed as byte data on odd addresses only. Address range FFFE00-FFFFFF selects the LSI Communication IC in the COMM Pack. Address range FE0000-FFFDFF selects the memory device (ROM) in the COMM Pack.

1260 (3000-Series) COMM Pack. For 1260 address information, refer to 1240 COMM Pack.

NOTE

For more information refer to Communication Pack Interface description *later in this section.*

Diagnostic LEDs. The LEDs can only be reached as supervisor data using the MOVES instruction (FC[0:2]=3).

Power Keep Alive. The Power-keep-alive can only be reached as supervisor data using the MOVES instruction (FC[0:2]=3).

Other GLUE Gate Array Operations. The specifics of GLUE gate array operation are described throughout the following MPU board functional descriptions. Refer to *Section 3: Connectors and Cabling* for an illustration that shows the GLUE gate array pin/signal assignments as viewed from the component side of the MPU board.

Read Only Memory. Refer to MPU Board Schematic Sheet 2 and the MPU Board Detailed Block Diagram in the *Section 11: Diagrams* when reading the following material.

Read-only memory consists of two 256 Kbit erasable programmable read-only memory integrated circuits (ICs) (EPROM); hereafter, referred to as ROM. These 32K by 8-bit ROMs store the instructions for setting up the microprocessor during power-on sequence, for running kernel tests, and for loading the operating system off the system disk. One IC stores the even-addressed byte KD[00:07] of a 16-bit word; the second IC stores all the odd-address byte KD[08:15] of a 16-bit word).

ROM functions are elementary. For example;

In read mode, both ROMs are addressed simultaneously. Thus, when the ROM/ signal goes active low, data at the ROM address is placed on the KD[00:15] data bus.

The EPROMs are programmed as follows: First, the ROMs are erased using an ultraviolet light source. This places all bits in the "1" state. (This is the only way to change a "0" to a "1".) Data can then be written by selectively writing "0" into the desired bit locations.

Diagnostic LEDS. Refer to the MPU Board Schematic 3 and the MPU Board Detailed Block Diagram in the *Section 11: Diagrams* when reading the following.

The Diagnostics LEDs reside in a single LED pack on the MPU. These LEDs are used to track the progress of the 68010 during the power-on process, indicating diagnostic codes as the microprocessor progresses through power-on diagnostic checks.

As the power-on routines progress, the LEDs indicate which test is being run. (The power-on sequence generally occurs too fast to be able to actually see a specific "power-on mode"; however, should the power-on procedure fail, then you may obtain some useful information. Lighted LEDs, in this case, contain information useful in determining the failed area. Refer to *Section 8: Troubleshooting*, for LED code explanations.)

The diagnostic LEDs monitor bits 0-7 of the kernel bus KD[00:07]. These bits are latched into the diagnostic LED by the LED signal from the GLUE gate array. A low on a data bit turns an LED on; a high turns it off. The latches are reset during the power-on sequence by IORESET/; therefore, all LEDs are turned on until an active LED signal latches in a new LED byte from the data bus. LED 9 is on during the active reset cycle; LED 10 is on during normal microprocessor execution.

2 Mbyte Random Access Memory. Refer to the MPU Board Schematics 5, 6, and 7 and the MPU Board Detailed Block Diagram in *Section 11: Diagrams* when reading the following material.

The compute kernel contains 2 Mbyte of DRAM for storing the operating system and for performing its designed applications. The primary purpose for DRAM is to store the operating system (pSOS) for running the 68010 microprocessor. Note that DRAM is not interfaced directly with the 68010, but rather through the GLUE gate array. Each time the MPU is turned on or is reset, the operating system is loaded into DRAM from the system disk (either floppy- or hard-disk). This is because the DRAM loses its data whenever power is removed.

RAM consists of sixteen, 1 Mbit DRAMs. This RAM is divided into two separately-addressable, 8-bit bytes. Thus, either a high-order or a low-order byte can be selected; or the microprocessor (via the GLUE gate array) can read all 16 bits simultaneously. Table 4-8 lists the RAM allocation and address locations for the 8-bit peripherals.

Table 4-8
Byte I/O Access Window Data Functions

Address	Data Function
844001–84401F	Serial I/O. For more information, refer to the Signetics Data Sheet for the SC2681.
845F01–845F07	Floppy disk controller. For more information, refer to the Western Digital Data Sheet for the WD1772.
844801–84483F	Real-time clock/calendar. For more information, refer to the Intersil Data Sheet for the ICM7170.
844401	Timer reset. This a write-only address that clears the timer interrupt any time it is accessed regardless of the data written.
844601	Floppy latch. This write-only address determines which drive is selected and which side of the disk is used. The bit assignments are as follows: Bit 0=Side 0/1 select Bit 1=Drive 0/1 select Bit 2=Not assigned Bit 3=COMM Pack Interrupt Polarity Control. Logic high indicates COMM Pack installed. Logic low indicates COMM Pack not installed.
844C01	Floppy status. This read-only address contains the status of floppy-disk drive readiness. The bit assignments are as follows: Bit 0=DISK_CHANGE Logic high indicates that a disk is inserted. Logic low indicates that the disk is removed. Bit 1=Drive 0/1 select Bit 2=Not assigned Bit 3=COMM Pack Interrupt Polarity Control. Logic high indicates COMM Pack installed. Logic low indicates COMM Pack not installed.

The following is a brief description of 2 Mbyte RAM operation.

Address Inputs. Twenty address bits are needed to address any bit location: 10 bits for the row address and 10 bits for the column address. First, ten row-address bits are provided at the LORA[0:9] input pins. These bits are latched into RAM with the low-active RAS (row address strobe) signal. Then, ten column-address bits are provided at the LORA[0:9] input pins and latched into RAM with the low-active CAS (column address strobe) signal.

Read/Write Enable. The read and write mode is selected with the RW signal. A logic high sets read mode. A logic low sets write mode. When the read mode is selected, the data input of the RAM is disabled. When write mode is selected, data output from the RAM is disabled.

Writing to RAM. The GLUE gate array addresses the bit location and data is then placed on the RID[0:15] bus. The GLUE gate array sets CAS1 and CAS2 to address the low and/or high order byte RAM. Figure 4-4 is a simplified schematic showing how this selection is made. Table 4-9 shows the relationship of DRAM control signals to high or low byte selection. Data is stored (written to RAM) on the falling edge of CAS00 and/or CAS01.

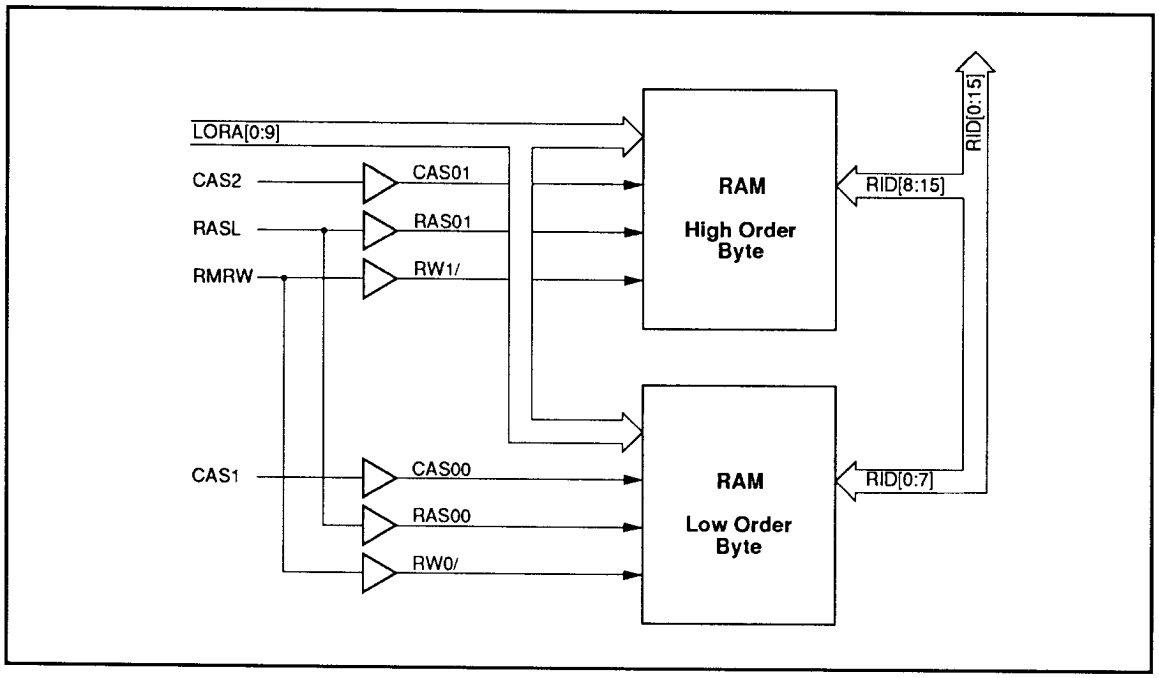


Figure 4-4. 2 Mbyte RAM buffering logic.

Table 4-9
High Order/Low Order Selection

DRAM Control Signals				DRAM	DRAM
RMRW	RASL	CAS2	CAS1	High Order	Low Order
X	low	Low	High	enabled	disabled
X	low	High	Low	disabled	enabled
X	low	Low	Low	enabled	disabled

Data Output (Read from RAM). As with data input, the GLUE gate array addresses the location of the bit to be read. When RW0 and/or RW1 is logic high (indicating read mode), data is placed on the data-out pin.

DRAM Refresh. Refresh of the dynamic memory cells is done by performing a refresh memory cycle on each of the A0-A8 row addresses at least once every 8 ms. Strobing each of the 512 row-addresses (A0-A8) with a falling RAS signal causes all bits in each row to be refreshed.

NOTE

During a reset, back-to-back refreshes occur. This results in an approximate 50% duty cycle for the RAS signal.

Low / High Byte Selection. As previously stated, low- and high-order byte selection is enabled by the CAS1, CAS2 signals from the GLUE gate array. These signals are set according to the logic state of the KLDS/ (Lower Data Strobe) and KUDS/ (upper data strobe) signals from the 68010 microprocessor.

NOTE

The "K" prefix indicates signals that are part of the critical kernel. That is, they are part of circuitry that must function for the MPU to execute any code. Buffered ("B") signals are not critical to the operation of the critical kernel.

The 68010 can simultaneously read or write all 16 DRAMS by activating both KLDS/ and KUDS/. This causes the GLUE gate array to enable both the CAS1 and CAS2, causing all bits of a 16-bit word to be written into or read from DRAM.

4 Mbyte Random Access Memory. Refer to the MPU Board Schematics 5A and 6A and the MPU Board Detailed Block Diagram in the *Section 11: Diagrams* when reading the following material.

The compute kernel contains 4 Mbyte of DRAM for storing the operating system and for performing its designed applications. The primary purpose for DRAM is to store the operating system (pSOS)for running the 68010 microprocessor. Note that DRAM is not interface directly with the 68010, but rather through the GLUE gate array. Each time the MPU Board is turned on or is reset, the operating system is loaded into DRAM from the system disk (either the floppy or the hard disk drive). This is because the DRAM loses its data whenever power is removed.

RAM consists of eight 1M by 4 bit DRAMs. This RAM is divided into four separately addressable, 8 bit bytes. Thus, the microprocessor (via the GLUE gate array) can select a high-order or a low-order byte from either the upper or lower 2 Mbyte bank of DRAM memory. The microprocessor can also read and write both high-order or low-order bytes in either bank of the memory simultaneously. Table 4-8 lists the RAM allocation and address locations for the 8 bit peripherals.

The following is a brief description of the 4 Mbyte RAM operation.

Address Inputs. Twenty address bits are needed to address any bit location in each bank of memory. The GLUE gate array uses RASL and RASH to select which bank of memory is used. Ten bits are used for the row address and ten bits are used for the column address. First, ten row-address bits are provided at the LORA[0:9] input pins. These bits are latched into RAM with the low-active edge of the RAS (row address strobe) signal. RASH is used for the upper 2 Mbyte bank of memory, and RASL is used for the lower 2 Mbyte bank. Then, ten column-address bits are provided at the LORA[0:9] input pins and latched into RAM with the low-active edge of the appropriate CAS (column address strobe) signal.

Read/Write Enable. The read and write mode is selected with the RW signal. A logic high sets the read mode, and a logic low sets the write mode. When read mode is selected, the data input of the RAM is disabled. When write mode is selected, data output from the RAM is disabled.

Writing to RAM. The GLUE gate array addresses the bit location, and data is then placed on the RID[0:15] bus. The GLUE gate array sets CAS1 to address the low order byte and CAS2 to address the high order byte in the lower bank of RAM. CAS4 addresses the low order byte and CAS3 addresses the high order byte in the upper bank of memory. Figure 4-5 is a simplified schematic diagram of the 4 Mbyte RAM showing how this selection is made. Table 4-10 shows the relationship of DRAM control signals to high or low byte selection. Data is stored (written to RAM) on the falling edge of CAS00 and/or CAS01 for the lower bank or CAS10 and/or CAS11 for the upper bank.

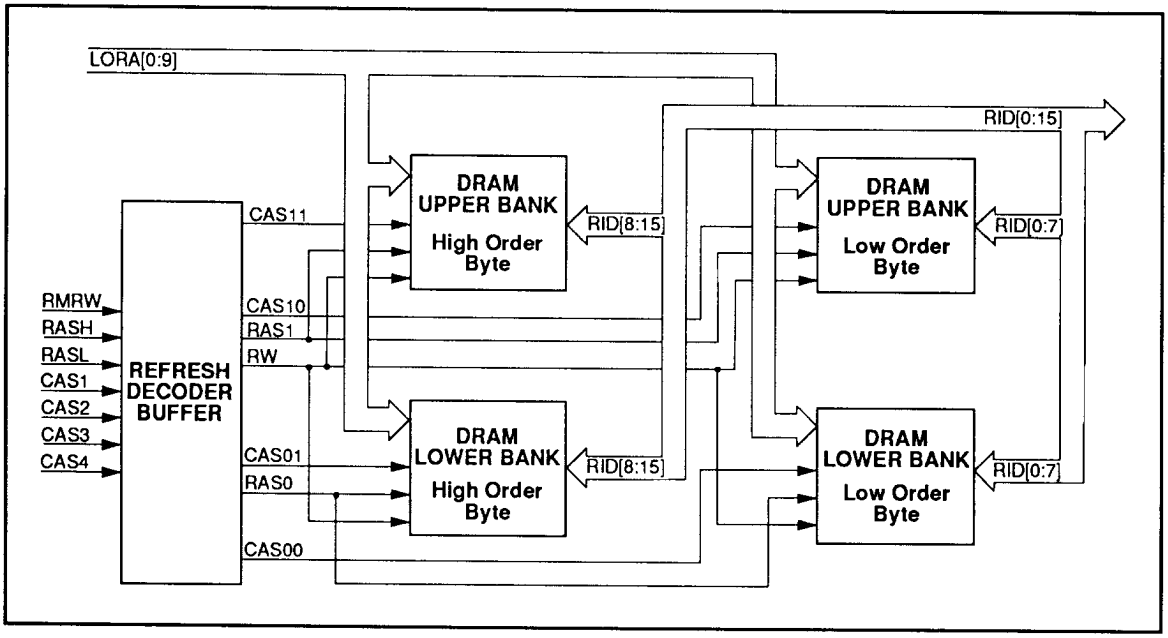


Figure 4-5. 4 Mbyte RAM logic.

Table 4-10
Upper/Lower Bank, High/Low Order Byte Memory Selection

DRAM CONTROL SIGNALS						DRAM			
						UPPER BANK BYTE ORDER		LOWER BANK BYTE ORDER	
RASH (RAS1)	CAS3 (CAS11)	CAS4 (CAS10)	RASL (RAS0)	CAS2 (CAS01)	CAS1 (CAS00)	HIGH	LOW	HIGH	LOW
high	high	high	low	high	low	disabled	disabled	disabled	enabled
high	high	high	low	low	high	disabled	disabled	enabled	disabled
high	high	high	high	low	low	disabled	disabled	enabled	enabled
low	high	low	high	high	high	disabled	enabled	disabled	disabled
low	low	high	high	high	high	enabled	disabled	disabled	disabled
low	low	low	high	high	high	enabled	enabled	disabled	disabled
low	X	X	low	X	X	refresh	refresh	refresh	refresh

Data Output (Read from RAM). As with data input, the GLUE gate array addresses the location of the bit to be read. When RW is a logic high (indicating read mode), data is placed on the data-out pin.

DRAM Refresh. Refresh of the dynamic memory cells is done by performing a CAS before RAS refresh memory cycle on the DRAMs. The GLUE gate array determines when to initiate a refresh cycle. A refresh cycle is started when both RASL and RASH go active low at the same time. The refresh decoder PAL detects this event then initiates a CAS before RAS refresh cycle in the DRAMs. In this type of refresh, the DRAMs contain a refresh address counter that cycles through 10 address bits (1024) of refresh addresses. A refresh cycle is needed on each refresh address at least once every 16 ms.

NOTE

During a reset, back-to-back refreshes occur. This results in an approximate 50% duty cycle for the RAS signal.

Low/High Byte Selection. As previously stated, low order and high order byte selection is enabled by the CAS1 and CAS2 (for the lower bank) and CAS4 and CAS3 (for the upper bank) signals from the GLUE gate array. These signals are set according to the logic state of the KLDS/ (Lower Data Strobe) and KUDS/ (upper data strobe) signals from the 68010 microprocessor.

NOTE

The "K" prefix indicates signals that are part of the critical kernel. That is, they are part of circuitry that must function for the MPU to execute any code. Buffered ("B") signals are not critical to the operation of the critical kernel.

The 68010 can simultaneously read or write all 16 data bits in each bank of DRAM by activating both KLDS/ and KUDS/. This causes the GLUE gate array to enable RASL, CAS1 and CAS2 for the lower bank or RASH, CAS4, and CAS3 for the upper bank, causing a 16-bit word to be written into or read from DRAM.

68010 Bus Buffers. Refer to MPU Board Schematic 2 and the MPU Board Detailed Block Diagram in *Section 11: Diagrams* when reading the following.

The 68010 Address bus is uni-directional. The Data bus is bi-directional. Both the address and data buses are buffered to provide isolation and to help drive the address and data lines to other devices that use the buses. (After buffering, the KD and KA bus signals are preceded by the letter B to indicate the buffering action.)

The bi-directional data bus provides the communication link between the microprocessor data bus and the other I/O functional devices on the bus. The following is a list of some functions performed using this bus:

- Read EPROM during the power-on process, to verify functionality of the operating kernel.
- Manage GLUE read/write communications with 68010 and other devices on the bus via the kernel data buffers.
- Report diagnostic LED status information.
- Manage data read/write bus for COMM Pack, hard disk, Video gate array, and TekLink gate array.

Control Signal Buffers. The MPU buffers the 68010 output control lines KLDS/, KUDS/, and KRW/. After buffering, these signals (now preceded by a "B") are used by various circuits for bus read/write control purposes. KLDS identifies data as bits 0-7; KUDS identifies data as bits 8-15. BBRW signifies either a read (active high) or write (active low) operation.

Interrupt Control. Refer to MPU Board Schematic 8 and the MPU Board Detailed Functional Diagram in the *Section 11: Diagrams* when reading the following.

A system device requests service of the processor by activating its respective interrupt request line. Because of the various interrupt sources, interrupt decoding and prioritizing is needed. This is done by the interrupt multiplexer and GLUE gate array logic.

Interrupt signals are input to high or low priority multiplexer ICs located in the interrupt multiplexer circuitry. The GLUE gate array continuously polls the multiplexers with the patterned PTR1, PTR2, and PTR3 signals. The result is an active-high INTH (interrupt high priority) or INTL (interrupt low priority) signal for each active interrupt request.

The INTH and INTL signals enter delay lines which effectively delay the signals one clock cycle. This delay ensures proper set-up and hold timing on entry to the GLUE gate array.

Because of the clock pattern of the PTR1, 2, 3 signals and the corresponding activation of INTH and/or INTL, the GLUE gate array restructures the interrupt acknowledge signals within its internal interrupt logic. Thus, it knows the exact source of the interrupt. The result is that IPL0/, IPL1/, and IPL2/ microprocessor interrupt inputs are set to represent the priority of the interrupt request.

The 68010 completes its current instruction, and, if no higher priority interrupts are pending, it acknowledges the interrupt by:

1. Setting the FC0, FC1 and FC2 outputs all high. (This actually informs the GLUE gate array that the microprocessor is servicing the interrupt.)
2. Setting KA[16:19] all high.
3. Placing the replication of the IPL0, IPL1 and IPL2 inputs onto address lines KA00, KA01, and KA02, respectively.
4. The GLUE Gate array responds with a vector number on KD[2:7]. KD bits 0 and 1 may be added by the interrupt source (such as the Video gate array); otherwise, they are logic high.
5. The 68010 multiplies the vector number by four to calculate the address of the interrupt routine. It then jumps to that address and begins executing.

DTACK Control. For most MPU operations, DTACK/ is controlled by the GLUE gate array. However, the bus cycle can be controlled by three other sources. These sources are: Hard Disk Controller board, Video gate array, and TekLink gate array. Figure 4-6 shows how alternate DTACK sources are controlled.

With BUN and PACK/ logic high, DTACKEN/ turns on buffer U513. The alternate DTACK sources are enabled, selecting a device which can provide its own DTACK signal. This circuit allows only one source to assert DTACK at a given time.

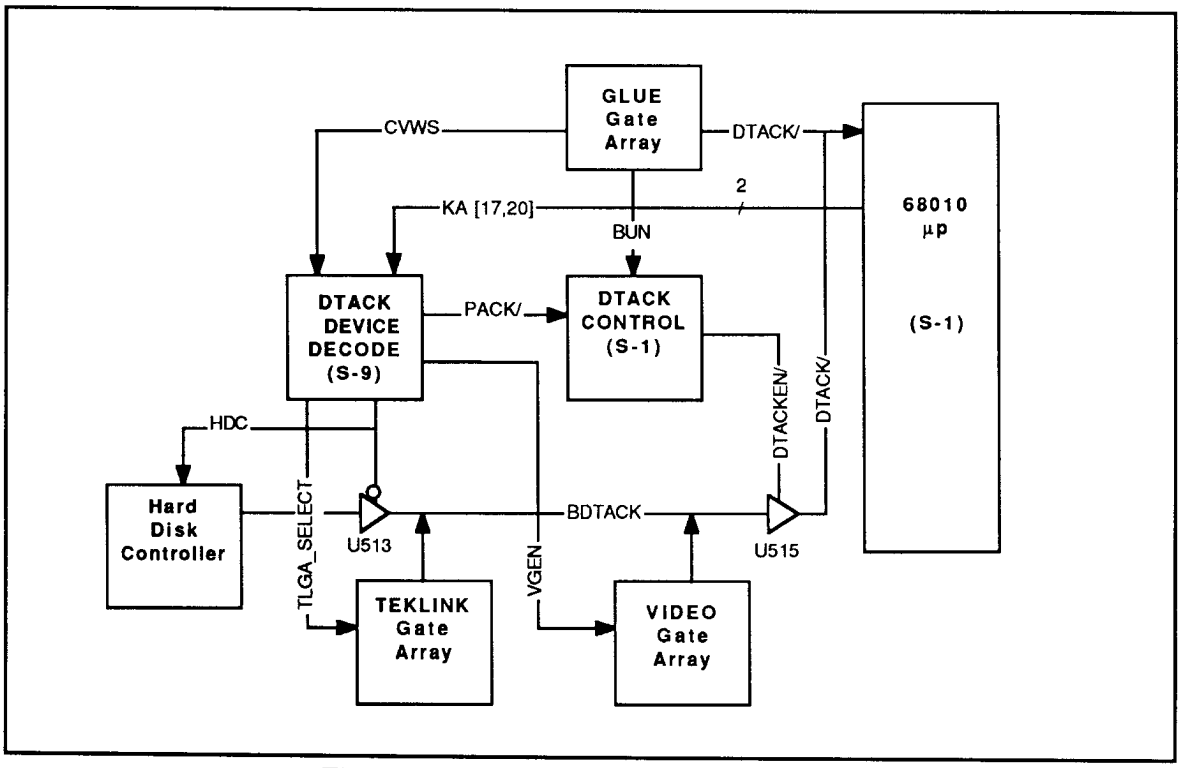


Figure 4-6. DTACK control block diagram.

Calendar (Real-time Clock). Refer to MPU Board Schematic 12 and the Detailed Block Diagram in *Section 11: Diagrams* when reading the following.

For time-keeping purposes, the MPU contains an Intersil 7170 real-time clock and associated circuitry. It uses the GLUE gate array IOD data bus for input/output.

The calendar IC is written to or read by accessing eight internal, separately-addressable counters which have the following functions:

- 0.01 (hundreds) sec.
- Second
- Minute
- Hour
- Day
- Date
- Month
- Year

An external 32 kHz crystal with trim capacitor C455 connects between the oscillator IN and OUT connections. (The command register, which is internal to the IC, is programmed for a 32 kHz crystal.) Address bits are GBA[1:2] of the GLUE address bus and BBA [3:5] of the buffered address bus. Refer to the Intersil 7170 data specification handbook for detailed information on address codes and corresponding calendar IC functions.

Read From Calendar. The content of the addressed calendar register is read to the IOD data bus when the CALENDARR signal goes low. CALENDARR is enabled when GBA bit 9 = 0, bit 10 =1, and bit 11 = 1.

Write to Calendar. A write to calendar is needed whenever the clock needs to be reset, due to time change, battery/power failure, etc. The contents of IOD data bus are read into the addressed calendar register when the CALENDARW signal goes low. CALENDARW is enabled when GBA bits 9 = 1, bit 10 = 1, and bit 11 = 0.

Use the Set Time/Date diagnostic routine to reset the calendar/clock.

Interrupts. The calendar IC can output two types of interrupts: periodic and compare. These interrupt signals are available at J460. However, they are not used for any circuit application other than adjusting the oscillator tuning. Refer to *Adjustment Procedures* for information on adjusting the calendar oscillator.

NOTE

For additional details on calendar Interrupts, refer to the Intersil ICM7170 Data Sheet Catalog.

Power Off and Battery Operation. Whenever the voltage between pin 14 and pin 13 is less than about 1 volt, the calendar IC automatically switches to battery backup operation. Until power is restored, operation is limited to timing, counting, and interrupt generation only. All other functions are disabled.

Beeper (Speaker) Control. Refer to MPU Board Schematic 3 and the MPU Board Detailed Block Diagram in *Section 11: Diagrams*.

The MPU board audio beeper circuit can be used by an application program to alert the user to key points in the application. An audio tone is generated as follows:

To generate an audio tone, the GLUE gate array outputs a BEEP signal. This signal is a square wave signal gated with a 40 kHz pulse-width modulated carrier. Volume is controlled by varying the duty cycle of the 40 kHz signal. (Refer to the *Beeper Control Latch* description under *GLUE Gate Array* for additional information.) Registers, within the GLUE gate array, can be preset by an application to provide programmable volume control.

The beeper, YG190, is driven by the field-effect transistor, Q285. Feedback resistor R286 provides quiescence bias, enabling the proper operation of the volume control feature.

The beeper circuit can be disabled by strapping pins 2 and 3 of J285, thereby grounding the gate of Q285.

The BEEP signal is routed to pin 1 of J285 for connecting to an external amplifier and speaker if desired.

Floppy Disk Interface

Refer to Schematic 10 and the Detailed Block Diagram in *Section 11: Diagrams when* reading the following.

Introduction

The primary interface component is a Western Digital 1772 Flexible Disk Controller/Formatter IC (hereafter called controller). All data communication to and from the MPU circuitry is via the IOD[00:07] bi-directional data bus and associated control lines. The data bus is used to transfer data, status, and control words (commands) out of or into the controller. The data bus lines are three-state buffered. They become output drivers when 1772_SEL is low and LBRW is high; they become input receivers when both 1772_SEL and LBRW are low.

During the power-on process, the IORESET/ signal is active low to set the controller and other floppy-disk drive control circuits to a known status.

Addressing the controller's registers is provided by GLUE address bits GBA[1:2]. GLUE address bits 9, 10, and 11, in conjunction with the LSIO and STDS signals, enable the 1772_SEL signal. The function decoder circuit also decodes the FDSELEN signal which latches the decoded SIDE I/O, DRIVE1, or DRIVE0 signals from the floppy-disk select register. An 8 MHz, 50% duty cycle clock signal from the GLUE gate array provides system timing.

Table 4-11 describes the 1772 Controller/Formatter IC input/output and signal control lines.

Table 4-11
WD1772 Input/Output Signals

MPU Signal	IC Symbol	IC Pin No.	Function
1772_SEL	CS/	1	Active low selects IC and enables communication with the device.
LBRW	R_W/	2	Logic high controls the placement of data on the IOD[00:07] lines from a selected register, while logic low causes a write operation to a selected register.
GBA[1:2]	A[0:1]	3,4	These two inputs with CS/ and R_W/ determine the internal register used for read/write as follows: **A1 A0 CS/ R_W/=1 R_W/=0** 0 0 0 Status Command 0 1 0 Track Track 1 0 0 Sector Sector 1 1 0 Data Data
IOD[00:07]	DAL[00:07]	5–12	Eight bit bi-directional bus used for transfer of data, control, or status. Enabled by CS/ and R_W/.
IORESET/	MR/	13	Logic low resets device and initializes the status register (internal pull-up).
GND	GND	14	Ground
+5 V	VCC	15	+5 VDC ±5% from power supply
STEP	STEP	16	Output pulse to the floppy disk drive for each step of the Read/Write head.
DIRECTION	DIRC	17	Output is high when stepping towards center of floppy disk, and low when stepping out.
8MHZCLK	CLK	18	Free-running 50% duty cycle clock for internal timing
RDATA	RD/	19	Active low input containing both clock and data pulses from the floppy disk drive
MOTOR_ON	MO	20	Active high output enables the spindle motor for read, write, or stepping operations.
WGATE/	WG	21	Output is valid prior to writing on floppy disk.
WRDATA	WD	22	Outputs clock and data pulses to write on the floppy disk.
TR_0	TR00/	23	Active low informs device when the Read/Write heads are over track zero (internal pull-up).
INDEX	IP/	24	Active low informs device when physical index hole on the floppy disk is encountered.

Functional Descriptions

The following explains how the floppy interface (primarily, the WD1772) performs basic input/output functions. Those functions are:

- Data transfer
  - -status and command register read/write
  - -disk read operation
  - -disk write operation
- Command operations
- Status register operation
- Double density formatting

Data Transfer (Read/Write). When the microprocessor requires data transfer with the floppy-disk, it addresses the controller. When the 1772_SEL signal goes low, the controller decodes the address bits GBA[1:2] . These address bits, together with the specific state of the LBRW signal (high = write, low = read) are interpreted by the controller to select the internal registers shown in Table 4-12.

Table 4-12
Addressing the 1772

GBA2	GBA1	LBRW=1 (HIGH)	LBRW=1 (LOW)
0	0	Status register	Command register
0	1	Track register	Track register
1	0	Sector register	Sector register
1	1	Data register	Data register

NOTE

Refer to the Western Digital Data Book for additional information on data transfer.

When GBA[1:2] are both low and LBRW is high, the contents of the controller's status register are placed on the IOD data bus. If LBRW is low, the content of the IOD data bus (a command byte) is loaded into the controller's command register.

To read from the disk, the MPU first loads the sector number into the controller's sector register. Next, the read sector command is issued. When the controller locates and verifies the data of the addressed sector, data loads serially into the controller from the RDATA line. After it is assembled in byte format in the controller's data register, the FLOPPY_DRQ line goes active high, causing the GLUE gate array to generate an interrupt, which the MPU services via the IOD[00:07] data bus. The MPU responds by addressing the controller's data register and setting the LBRW bit high to place the data byte on the IOD bus. Following the read of the data register, the FLOPPY_DRQ lines goes low. This process repeats until the end of sector is reached.

To write to the disk, the MPU first loads the sector numbers into the controller's sector register. The MPU then issues the write sector command. When the controller locates and verifies the addressed sector, it generates an active-high FLOPPY_DRQ signal. This signals the MPU to place a data byte on the IOD[00:07] data bus and switch the LBRW line low. This action latches the data into the controller's data register, causing the FLOPPY_DRQ signal to go inactive low. The controller then activates the WGATE signal to the floppy-disk, writing the data into the data field on the disk.

The preceding process repeats until all data has been clocked out of the data register and written on the disk.

NOTE

Writing is inhibited when the WPROTECT/ (Write protect) input is logic low. In this case, any Write command is immediately terminated, an interrupt is generated (FLOPPY_IRQ), and the write protect status bit (of the controller's status register) is set.

Command Operations. The controller can accept 11 different commands. These commands and their respective bit assignments are shown in the Western Digital data book for the 1772 Controller/Formatter IC. All commands contain bits that have variable assignments depending on the desired command activity. Again, if additional information is needed, refer to the Western Digital data book for the 1772 Controller/Formatter IC.

NOTE

The assigned state of a variable bit is application-dependent. Their assignments are preset by the system software and normally will not be changed from their assigned states.

Refer to the Western Digital Data Book for detailed descriptions of each command operation.

Status Register Operation. Table 4-13 shows the bit assignments for the status byte. Upon receipt of any command (except the force interrupt command), bit 0 is set and the other status bits are updated, or cleared, for the new command. The busy status bit also controls the FLOPPY_IRQ signal. When the 1772 floppy system is busy, this signal is active. The MPU monitors this signal to determine when a floppy-disk command operation is completed.

Table 4-13
Status Bit Assignments

Bit	Name	Meaning
IOD07	Motor On	This bit indicates the status of the Motor On output.
IOD06	Write Protect	On Read Record: Not used. On Read Track: Not used. On any Write, it indicates a write protect. This bit is reset when updated.
IOD05	Record Type/Spin-Up	When set, this bit indicates that the motor spin-up sequence has completed (5 revolutions) on Type 1 commands. For Type 2 and Type 3 commands, this bit indicates record Type. 0 = Data Mark; 1 = Deleted Data Mark.
IOD04	Record Not Found	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
IOD03	CRC Error	If S4 is set, an error is found in one or more ID fields; otherwise it indicates an error data field. This bit is reset when updated.
IOD02	Lost Data/Track 00	When set, it indicates the MPU did not respond to DRQ in one byte time. This bit is rest to zero when updated. On Type 1 commands, this bit reflects the status of the TRACK00 signal.
IOD01	Data Request	This bit is a copy of the DRQ signal. When set, it indicates the Data Register is full on a read operation or empty on a write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the INDEX signal.
IOD00	Busy	When set, it indicates that a command is being executed. When reset, no command is being executed.

If a force interrupt command is received when there is a current command under execution, the BUSY status bit is reset, but the rest of the bits are unchanged. If the force interrupt command is received when there is not a current command being executed, the BUSY bit is reset and the other status bits are cleared.

NOTE

When the data register is read to the IOD data bus the DRQ bit in the status register and the DRQ output (FLOPPY_DRQ) are automatically reset. A Write from the IOD bus to the data registers also causes the same actions.

Double Density Formatting. As stated earlier, the floppy disk is double-density formatted with 256 bytes per sector.

To format the disk, the controller receives the write track command, causing the busy status bit (bit 0) in the status register to be set. The formatter/controller ICs data register is loaded with the values shown in Table 4-14. For each byte to be written, there is an active data request (FLOPPY_DRQ) signal to the MPU.

Figure 4-7 shows the track/sector format and the relationship of the INDEX pulse and the WGATE (write gate) signals.

Table 4-14
Floppy Disk Track and Sector Format Contents

Number of Bytes	Hexadecimal Value of Byte Written
60	4E
12*	00
3*	F5 (Writes A1)
1*	FE (ID Address Mark)
1*	Track Number (0 thru 4C)
1*	Side Number (0 or 1)
1*	Sector Number (1 thru 1A)
1*	01 (Sector Length)
1*	F7 (2 CRCs written)
22*	4E
12*	00
3*	F5 (Writes A1)
1*	FB (Data Address Mark)
256*	Data
1*	F7 (Data Address Mark)
24*	4E
668†	4E

**The formatting sequence writes these fields 16 times.*
†*Continues writing until Controller interrupts out (≈668 byte).*

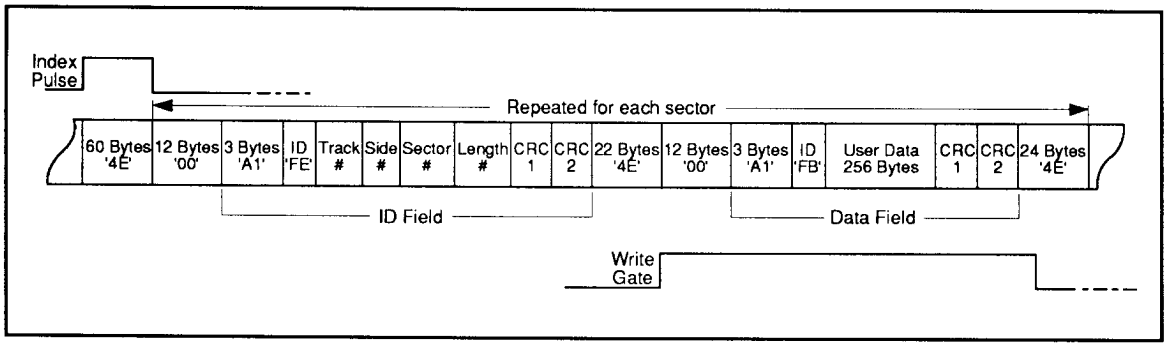


Figure 4-7. Floppy disk track and sector format.

Video Controller

Introduction

Refer to MPU Board Schematics 9, 13 and 14, and the MPU Board Detailed Block Diagram in *Section 11: Diagrams* when reading the following.

The video controller consists of the video gate array and video RAM. This circuitry functions as a powerful display engine that can drive color and monochrome CRTs, or a flat-panel display. Regardless of the display device, data is displayed on a grid 640 pixels wide by 400 pixels high.

The video gate array provides the hardware that drives the display device. It includes circuitry that identifies the type of display attached (color CRT, monochrome CRT, or flat panel) and then modifies the video output and control signals to drive the attached monitor.

Display RAM serves two functions:

1. A 32K by 8 section provides a bit map of the displayed image for graphics (waveform) display. Two 32K x 8 ICs provide 2:1 mapping (two bits per IC for color display).
2. An 8K by 8 section stores image information for up to 256 displayable text characters.

The following list of video controller functions are described:

- Video output
- Operating modes
- Display memory
- Display RAM access cycle
- Screen copies
- Video gate array pin assignments

Video Output

As stated in the introduction, the video gate array supports either a color CRT, a monochrome CRT, or a flat-panel display. The same display output connector is used to connect to the color CRT and flat-panel display external to the mainframe; only the interconnect cable is different. If a monochrome CRT is used, the video controller is hard-wired to the CRT internal to the mainframe. There is no external Display/Monitor connector. (Refer to the applicable mainframe service manual for MPU board-to-display-interconnect drawings and related information.)

Table 4-15 shows the pin/signal assignments of the display controller output connector, J820. This connector is used to connect to an external color video CRT or flat-panel display. The MPU board used in a PRISM 3001 or 2505 TestLab mainframe does not have an external display connector. It connects directly to a monochrome CRT mounted internal to the mainframe. Refer to the applicable mainframe service manual for details regarding signal interconnect. Signal descriptions are provided in *Section 13: Glossary.*

Table 4-15
Display Controller Output Connector, J820

Pin	Signal
1	+12 VDC (for flat panel)
2	GND
3	VSYNC
4	GND
5	HSYNC
6	GND
7	VID0 (monochrome)
8	GND
9	VID1 (blue)
10	Not used
11	VID2 (green)
12	Not used
13	VID3 (red)
14	GND
15	VCLK (for flat panel)
16	GND
17	Not used
18	GND
19	TOUCH_H
20	TOUCH_L
21	+12 VDC
22	+12 VDC
23	+12 VDC
24	+12 VDC

CRT Video Operation. The TOUCH_H and TOUCH_L signals are monitored by the video gate array to determine whether a color CRT or flat-panel display is attached. When a color CRT is attached, these lines are both high. The video gate array then configures its operation to drive the RGB display. Figure 4-8 shows the timing and data transfer protocol for a video monitor. Note that pixel data is output bit-serially, one raster line at a time.

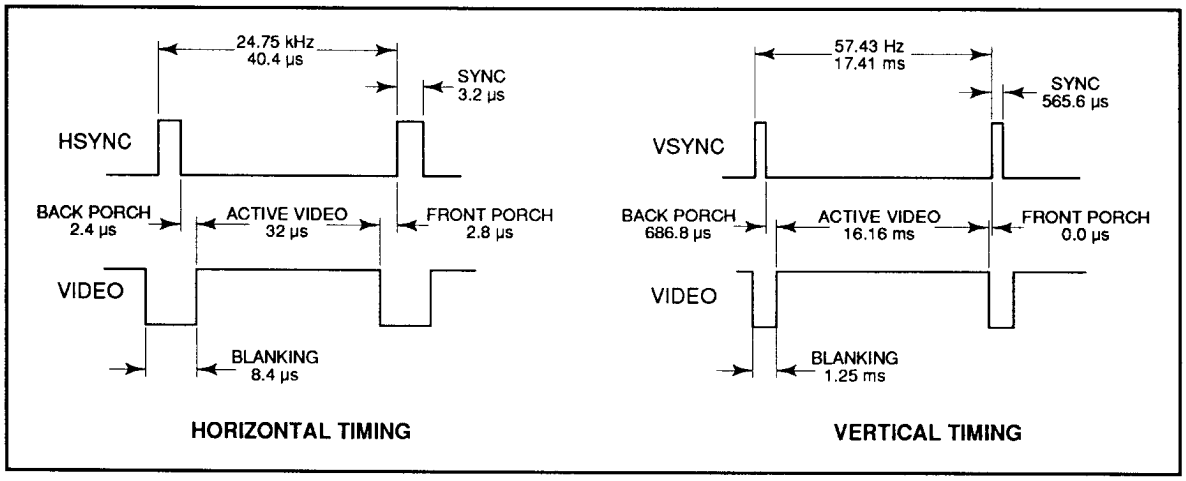


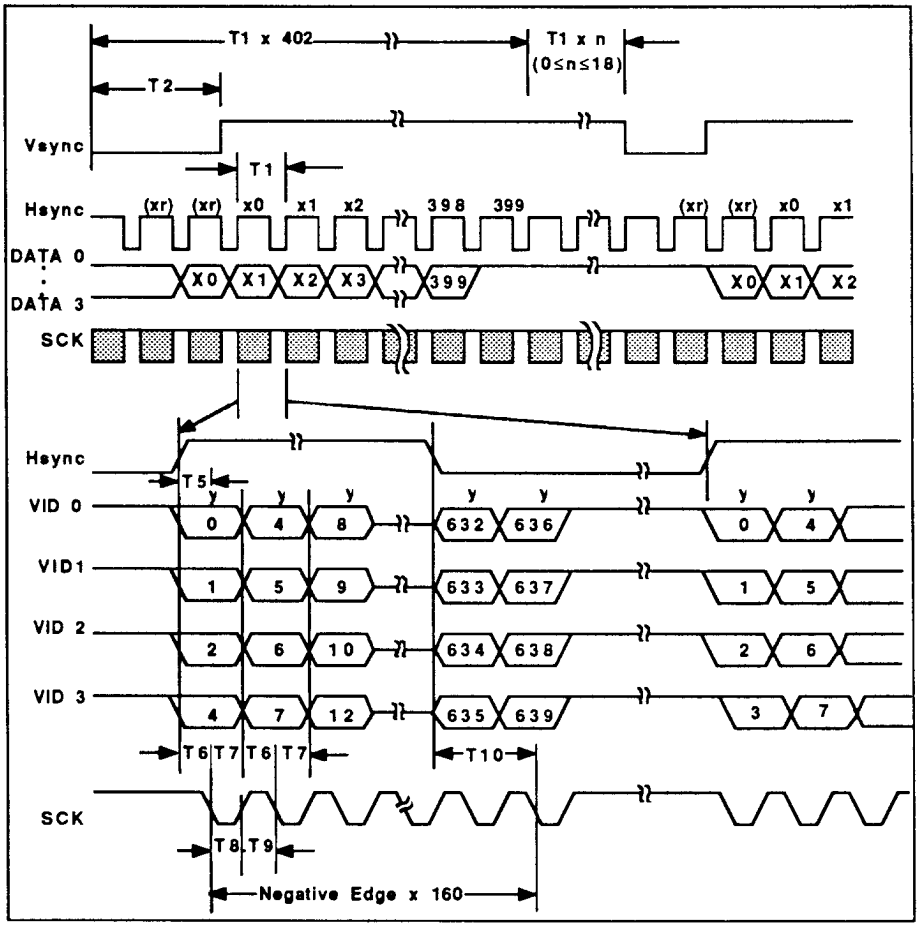
Figure 4-8. Video timing and control signals

The video gate array drives both the RGB and MONOCHROME signals whenever a color or monochrome CRT is installed. Interconnect cabling and plugs ensure that the appropriate signals are routed to their respective video monitors. (The MPU board used in the PRISM 3002 Series or the 2510 TestLab mainframes includes an external Display/Monitor connector for driving either a color monitor or a flat-panel display. The MPU board used in the PRISM 3001 or 2505 TestLab mainframe does not include this external connector, but is hard wired to a CRT monitor internal to the mainframe. Refer to the *Diagrams* section in the applicable mainframe service manual for display interconnect details.)

The power-on boot ROM loads the pre-determined display "values" into SYNC-control registers in the video gate array. The content of these registers controls the horizontal blanking, vertical blanking, and retrace intervals. The content of these registers also select between serial or parallel transmission of pixel information to the display. (Video CRTs receive pixel information serially, one horizontal scan line at a time. The flat panel can receive and display pixel data up to four lines at a time. Flat panel operation is described more completely under *Flat Panel Operation.)*

Flat Panel Operation. If the Flat-Panel Display module is connected, the TOUCH_H and TOUCH_L signals will be complementary. The Video gate array configures its operation to drive the flat-panel display. Figure 4-9 shows the timing and data transfer protocol for the flat-panel display. Note that pixel data is output bit-serially, four raster lines at a time, on lines VID0-VID3.

The flat-panel display receives +12 VDC from the MPU board to power the flat-panel display. It also receives the VCLK signal for timing the display circuitry.



	Min.	Max.	Unit
T1*	39.6	41.7	µs
T2	10	12	µs
T3	40	160	µs
T4	-5	5	µs
T5	-100		ns
T6	20		ns
T7	100		ns
T8	90		ns
T9	90		ns
T10		6.5	µs

*Refresh Cycle:

T1 = 39.6µs → $\frac{1}{420 \times 39.6 \times 10E\text{-}6}$ =60 Hz

T1 = 41.7µs → $\frac{1}{420 \times 41.7 \times 10E\text{-}6}$ =57 Hz

Figure 4-9. Flat panel video timing and control signals.

Operating Modes

NOTE

The video gate array is a custom gate array device that manages all display controller functions. A technician can easily treat the array as a "black box" ignoring what occurs inside the array. However, a good understanding of how the video gate array uses video RAM and windowing concepts is necessary for efficient troubleshooting of the video controller circuitry.

Physical Windows. The video gate array segments the display into physical windows as shown in Figure 4-10. Two text windows support smooth vertical scrolling (smooth scrolling is the ability to shift an entire image in increments of one pixel line at a time). These two windows are scrolled independently by using their own pixel-row offset registers (these registers are part of the VGA).

A graphic window can be turned on in each of the smooth scrolling text windows. (The graphic window is used to display waveforms, cursors, and text.) When turned on, the graphic window extends from character column 16 (on the left side of the display) to character column 79 (on the right side of the display). The graphic window extends from the top scan row to the bottom scan row of the scrolling window.

NOTE

The graphics windows are scrolled independently by their own offset registers. These registers control the number of pixels by which the graphic image is shifted either horizontally or vertically.

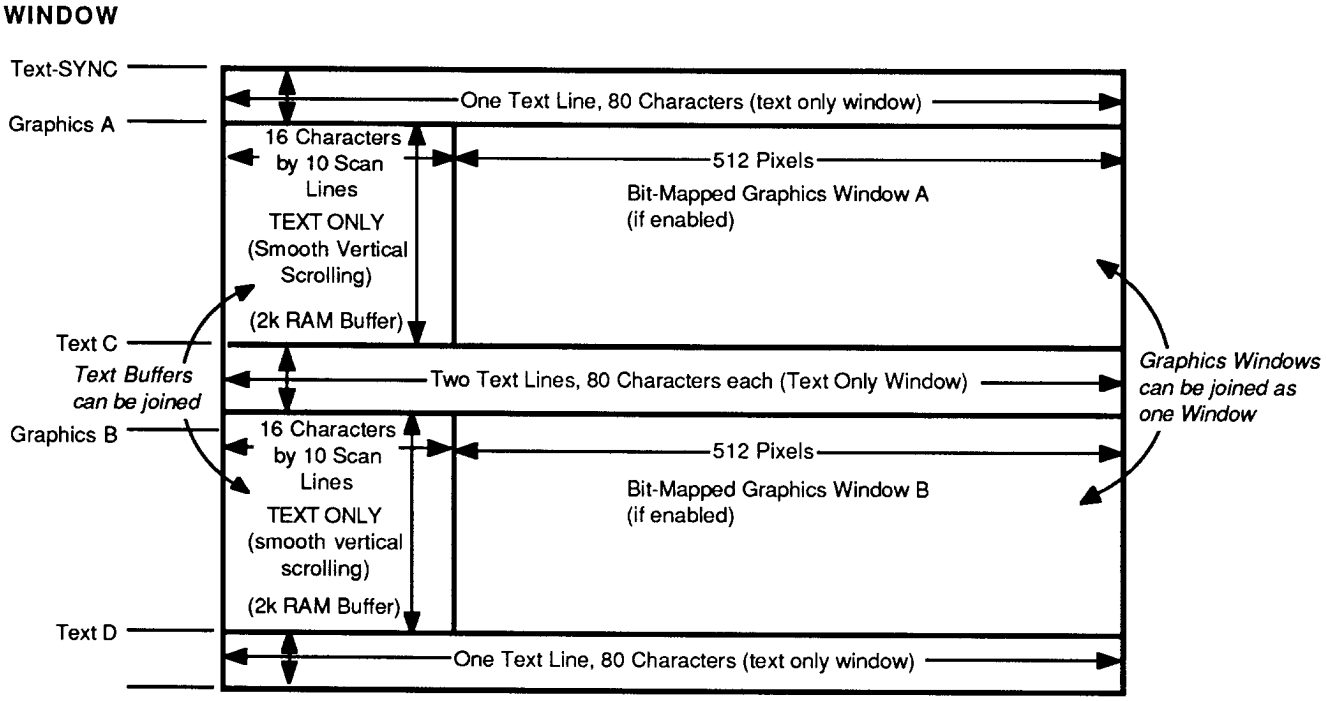


Figure 4-10. Example of display window.

Data Windows. "Data windows" refers to the memory space that stores the data to display in one of the physical windows on the display screen. The video gate array manages hardware windowing by:

- Locating the top scan line of a display area (window) on the physical display, and
- Locating the source (memory location in Video RAM) of the data that will be displayed in the physical window.

Figure 4-11 is a memory map. This illustration also shows the correlation between memory locations and the display windows.

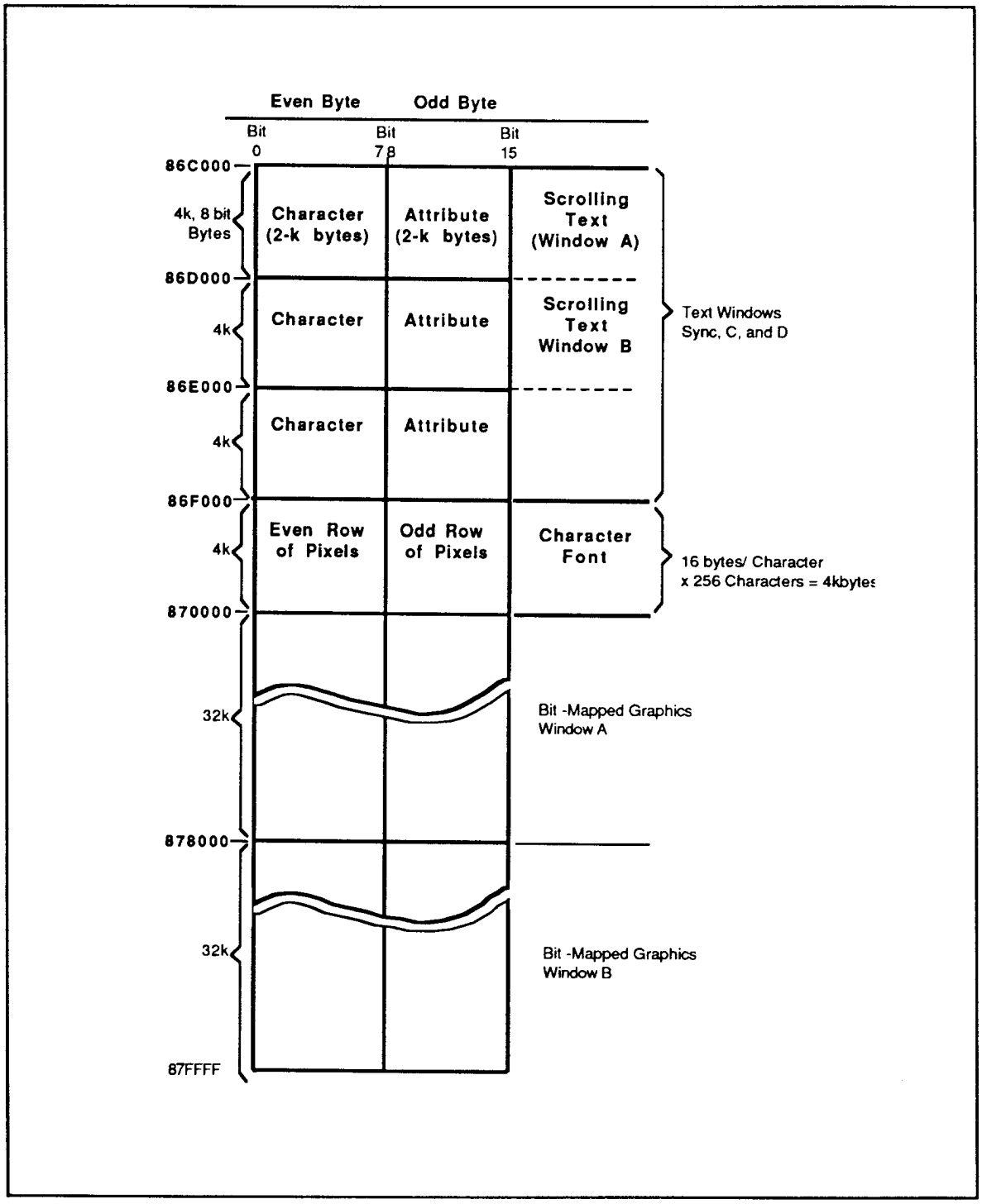


Figure 4-11. Video RAM memory map showing correlation between memory addresses and display windows.

The video gate array manages data windowing by using two smooth-scrolling window buffers. These are "circular," 2 Kbyte buffers that wrap around when the 2 Kbyte (end of buffer) boundary is reached. Depending on the user interface (application), these buffers can be joined into a single 4 Kbyte buffer with two pointers to it.

The other three text windows (C, D, and E) use a single 2 Kbyte text buffer. This buffer overlaps the 4 Kbyte contents of the smooth-scrolling windows. That is, they can use the memory allocated for windows A and B (2K + 2K = 4K).

Bit-Mapped Graphics Windows. The video gate array displays graphic images (waveforms with text labels in the adjacent, smooth-scrolling text windows). The physical location of these graphic windows is shown in Figure 4-10.

NOTE

When reading this information, please keep in mind that the Video Gate Array is configured by the MPU System and Application system software.

The video gate array contains a hardware drawing machine that draws data points, draws risers (vertical lines connecting data points), and copies character images from the font memory for display in the bit-mapped window. This drawing engine frees the MPU from having to perform the mundane and time-consuming tasks associated with bit-mapped graphic display images.

NOTE

When drawing images into the bit map, the drawing machine automatically uses the color attributes (stored in the drawing engine's command register) for the new image. The colors that are displayed are determined by the color look-up table in the color register.

Display Memory

As previously stated, the video gate array is supported with 80 Kbyte of RAM. This RAM is mapped as shown in Figure 4-11. This memory is contained in two 32K x 8 (256 Kbit) and two 8K x 8 (64 Kbit) ICs. These ICs are shown on the Schematic, Sheet #13 in *Section 11: Diagrams*. The 32 Kbyte RAM ICs are used for bit-mapped graphic displays; the 8 Kbyte RAM ICs are used for storing of character font tables and text characters.

The following information describes how text and bit-mapped graphics RAM are used by the video gate array.

Character Font Memory. The character font memory space is mapped in Figure 4-11. It stores pixel information for up to 256 characters.

When the mainframe is powered on, the pixel representation of the 8-bit character code is read from microprocessor ROM and stored in font memory. The pixel information for each character is contained in eight 16-bit words that are stored in a 16-bit by 8-bit character matrix as shown in Figure 4-12. A character occupies a "cell" within the pixel matrix. There are two character cell sizes; normal text and label text:

- Normal text cells are 10 pixels high by 8 pixels wide.
- Label text cells are 16 pixels high by 8 pixels wide. (Label characters are characters displayed to the left of the graphic windows.

Figure 4-12 shows how pixels are stored and displayed for the ampersand (&) character, normal font. Note that each 14-bit word, in the font storage cell, contains two lines of pixel information. A character matrix is stored in character font RAM in byte order; 86FXX0 is the top row, 86FXX1 is the next row down, and 86FXXF is the bottom-most row of the character matrix.

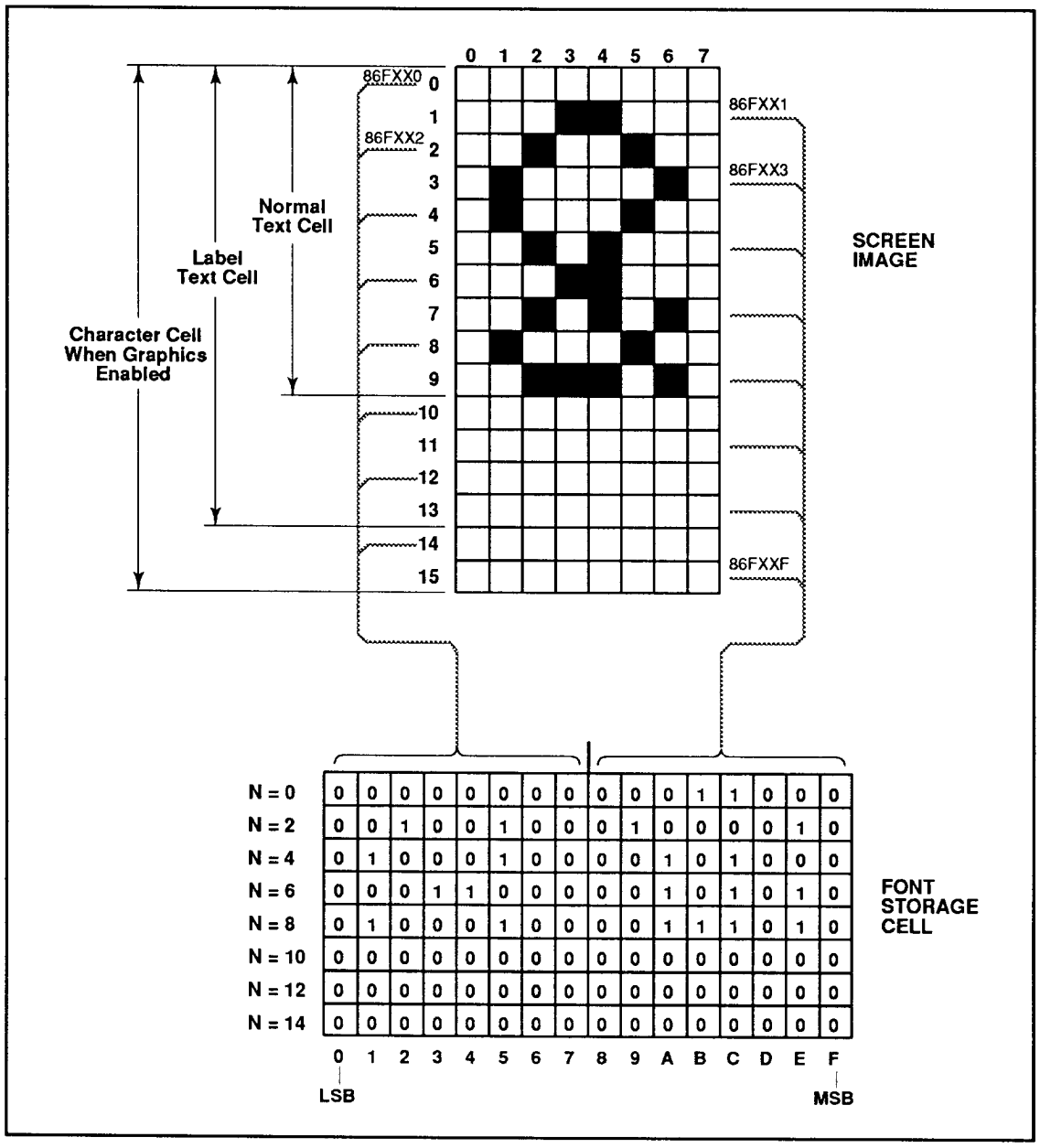


Figure 4-12. Relationship of displayed character to font memory.

Text Memory. During the power-on boot process, the font code for the character set used by the MPU is read from boot ROM and loaded into display RAM. Each displayed character is stored using an 8-bit character code and an 8-bit attribute code. Thus, each character occupies 16 bits in text memory. (See Figure 4-13.) Note that the attribute code is used to assign attributes to the character as shown in the illustration.

NOTE

The color attributes are not used for a flat-panel display.

MPU "block moves" the contents of the font ROM to the display RAM between 86F000 and 86FFFF. When the MPU wants to display a character, it places the desired character code and attribute in a memory location somewhere between 86C000 and 86EFFF, as determined by the choice of windowing.

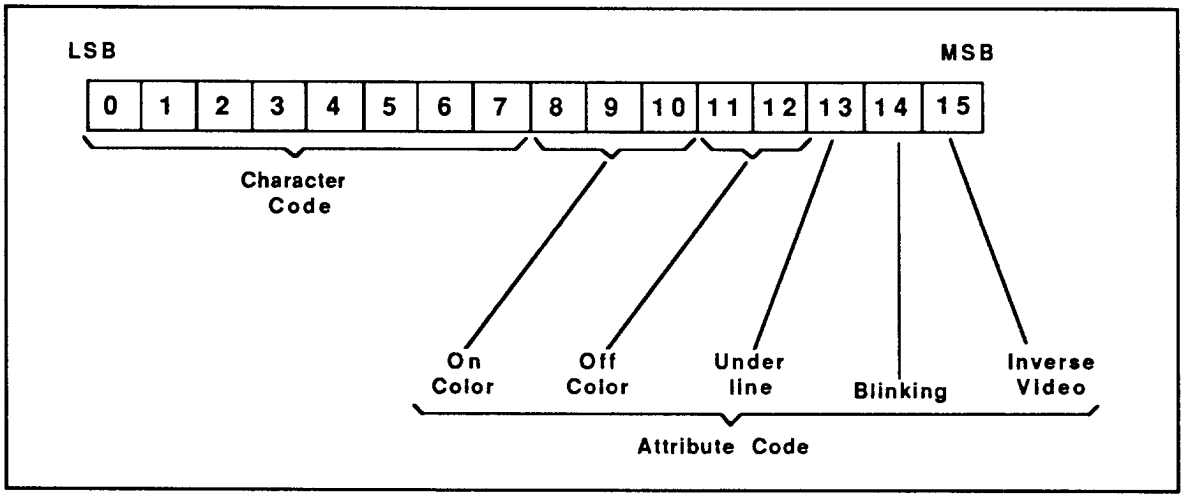


Figure 4-13. Text character storage and attribute codes.

Reading Text Memory. Refer to Figure 4-14. Text characters are read from text memory as follows:

1. Based on data from the MPU (the user interface application stored in registers in the video gate array), the video gate array identifies the address of the character to be printed on the display screen and determines the display window (screen location) in which the character will be printed.
2. The video gate array retrieves the 16-bit code for the desired character. It places the 8-bit character and 8-bit attribute codes in separate registers.

3. Using both the 8-bit character code and the current scan line to address the font location in font RAM, the video gate array searches through the font matrix. This results in a string of eight pixel bits loaded into the Video gate array.

   On successive scan lines, the video gate array increments the character scan line value by one line, selecting a set of pixels that are separated from the physical address of the first font value by 1 byte (8 bits).

4. The video gate array modifies the pixel data as determined by the character attribute code stored in the attribute register, then delivers the pixels to the display device (using the method appropriate for the attached display device). For example, if a color CRT is used, then color attributes are added and the pixel data is transmitted to the display in a serial string, one raster line at a time. If a flat-panel display is used, then the video gate array transmits four raster lines of pixel data, bit serially, ignoring the color bits of the attribute code.

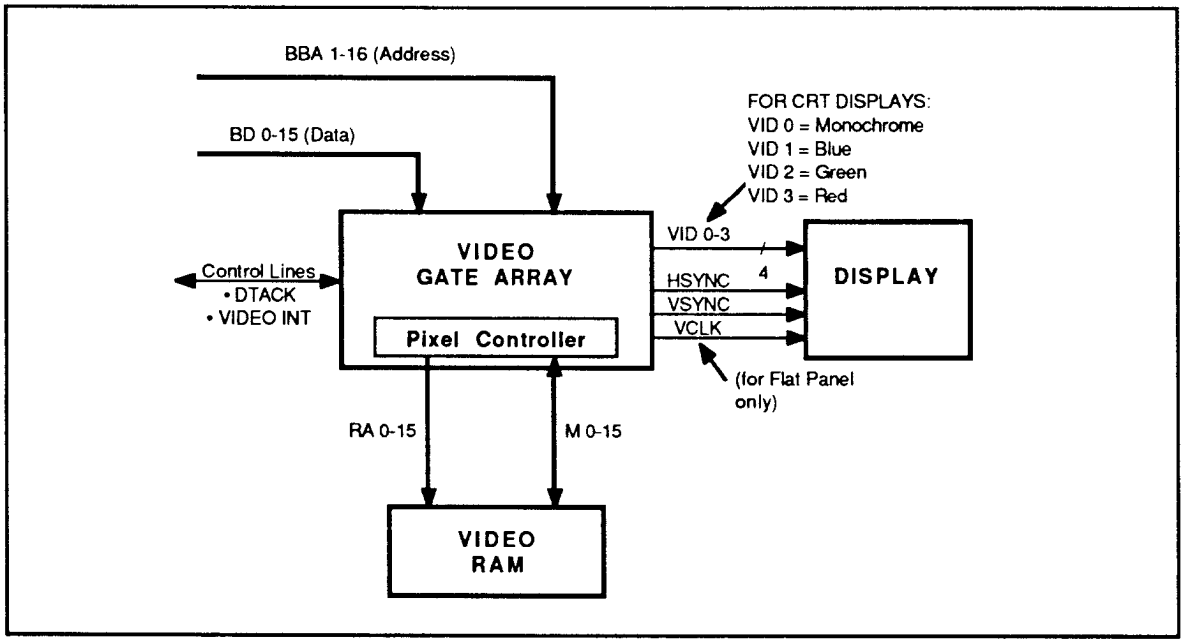


Figure 4-14. Simplified diagram showing data flow from video memory to display.

Graphics Memory. Graphics memory consists of two 32K by 8 bit memory ICs whose memory address space is mapped in Figure 4-11. This memory functions as a bit map in which pixel data is stored for the image displayed in a graphics window.

The color display requires two bits of information for each pixel displayed. Pixel information is stored in graphics memory in 16-bit words. Each word contains pixel color information for 8 bits, as shown in Figure 4-15. A color look-up table is used to convert the two bits for each pixel into the three signals going to the color CRT.

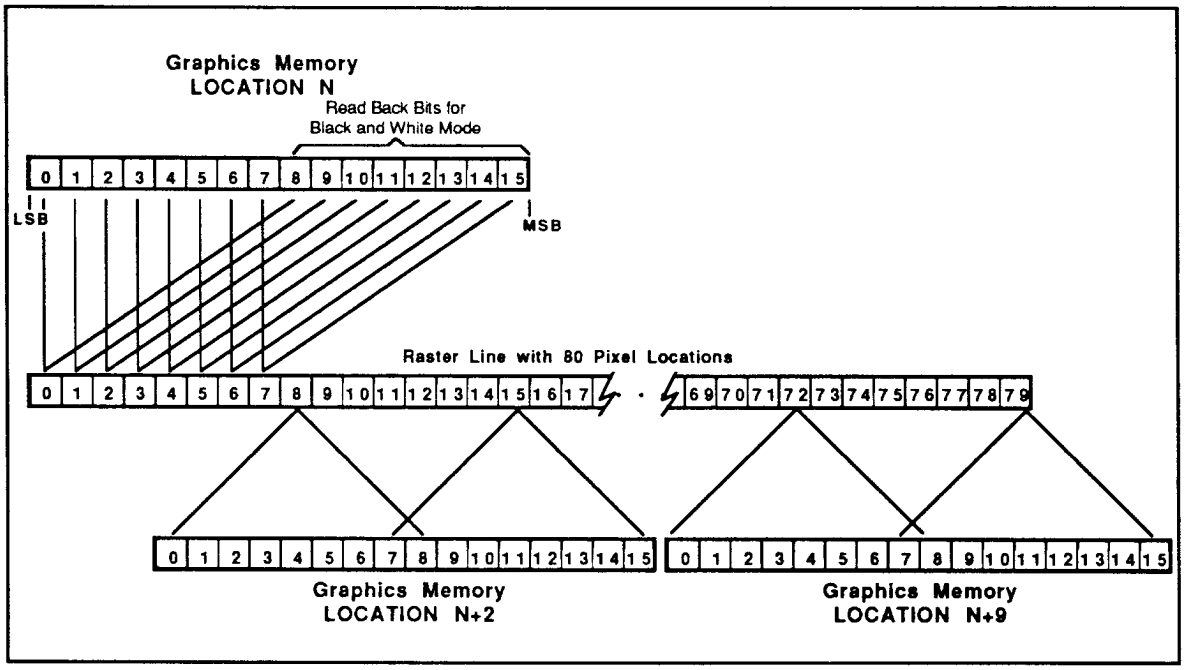


Figure 4-15. Graphics image translation from RAM data bits to display bits.

Display RAM Access Control

The video gate array uses the following bus cycles for text and graphics mode. Both modes have an access cycle that is 16, clock cycles long as shown in Figure 4-16.

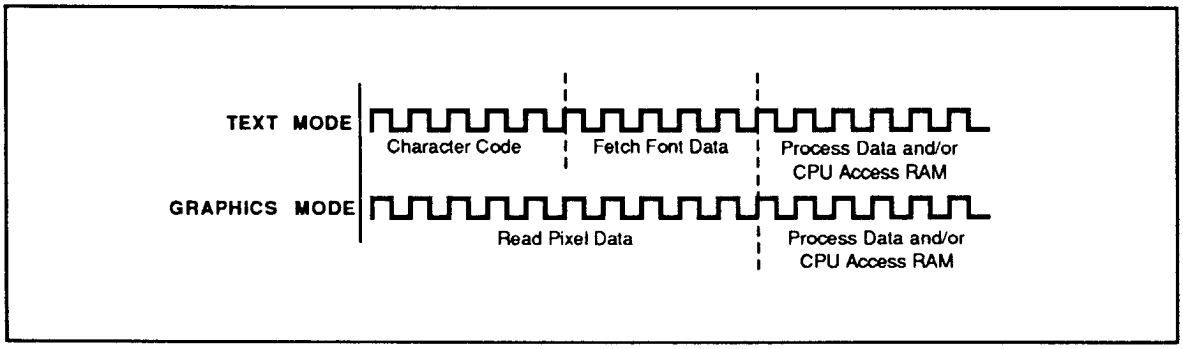


Figure 4-16. Video gate array bus cycle.

Text mode uses five clocks to read the addressed character code from the text font RAM, and another five clocks to fetch the display data from the character font (based on the read character code).

The graphics bus cycle uses 10 clocks to read the addressed graphics pixels from the graphics RAM.

Both text and graphics bus cycles allow 6 clock cycles for the video gate array to draw the data (if so commanded), and/or for the MPU to access display RAM (text or graphics RAM).

Screen Copies

When commanded to generate a screen copy, the video gate array copies an 8 by 8 pixel cell as the pixels are being delivered to the display. It copies this cell into a register array and then generates an interrupt to the MPU, indicating that the data is available. The MPU then reads the register array, and routes the image data to the screen output software. The process repeats until the entire display has been copied. (This screen read-back is compatible with Epson® RX80 operation.)

NOTE

Color images cannot be copied. The MPU/video controller circuits provide black and white data only.

Video Gate Array Pin Assignments

Section 3: Connectors and Cabling contains an illustration that shows the pin and signal assignments for the video gate array, as viewed from the component side of the MPU board.

Keyboard and Host Interface

Refer to MPU Board Schematic 11 and the Detailed Block Diagram in the *Diagrams* section when reading the following.

Introduction

The MPU board uses a Signetics 2681 DUART (and other GLUE logic) to interface with a keyboard (or control panel) and an RS-232-C host. Figure 4-17 shows the DUART data channels. The 2681 is a two-channel integrated circuit; channel A is the keyboard (control panel) interface and channel B is the host interface. Both channels are full-duplex asynchronous. The DUART contains a 7-line input general-purpose port and an 8-bit general-purpose data output port. Both ports can be used for miscellaneous control and communication functions. The 2681 accepts a baud clock from the GLUE gate array, and it provides interrupt control and operational control for the read, write, and address decoding functions. Address decoding is done using the GLUE bus address bits GBA[1:2], and buffered address bits 3 and 4.

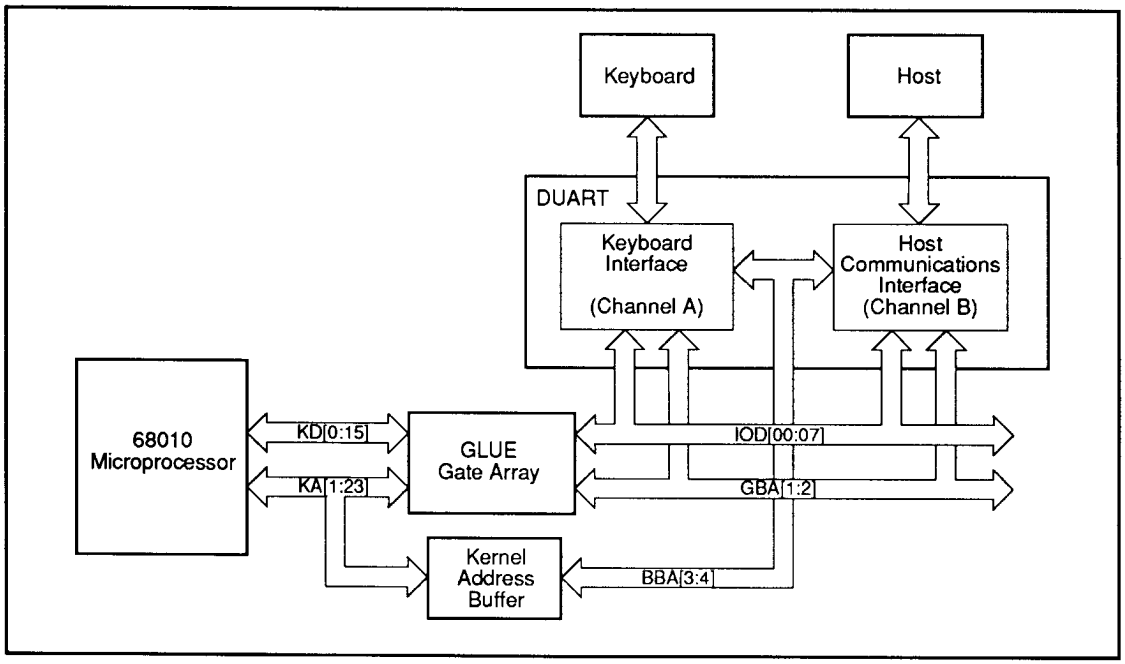


Figure 4-17. DUART data channels.

The keyboard and control panel interface (hereafter referred to as keyboard) is described first, followed by a description of the host interface.

Keyboard (Control Panel) Interface

The keyboard interface circuitry provides data input/output control between the MPU board and any connected control panel/keyboard or RS-232-C device.

The following provides a brief description of how the DUART and associated circuitry transmits data to and receives data from either a keyboard or a control panel via the GLUE IOD data bus.

Serial data is transferred from the keyboard to the DUART at a sustained transfer rate of 19,200 baud (the KEY.CLOCK signal). Thus, received keyboard data is fully synchronized with KEYCLOCK.

When conditioned to receive data from the keyboard (or control panel), the 2681 looks for a high to low (mark-to-space) transition of the start bit on the RXA input pin. When a transition is detected, the state of this pin is sampled for the next 7½ cycles of KEYCLOCK. After the data from the keyboard is clocked into the DUART, one bit at a time, the data is then transferred to a receive holding register in the DUART. This triggers the DUART to activate the IRQ (interrupt request) and KBTRANINT (keyboard transmit interrupt) signals. This informs the GLUE gate array that the DUART has keyboard data. When the MPU is ready to receive the data, it sets the RDN line active low (via the function decoder circuit and the GLUE gate array). This causes the contents of DUART to be presented on the IOD data bus.

NOTE

The read cycle begins on the falling edge of RDN.

MPU Handshake Protocol. The following describes the basic implementation of the keyboard-to-MPU handshake protocol.

The GLUE interrupt logic first samples the DUART register lines (IRQ, etc.) to determine if the DUART is busy. When the keyboard is able to accept data from the DUART, the KBTRANINT (Keyboard Transmit Interrupt) line will be high. GLUE interrupts the CPU, after which the CPU writes the command into the DUART, places a data byte (keyboard command data) on the IOD data bus, addresses the DUART, and then sets the WRN high. On the rising edge of WRN, data is clocked into the DUART. The DUART transmitter converts the data to a serial stream that is clocked to the keyboard at a 19.2 kHz internal clock rate.

Data from the keyboard is clocked into the DUART by KEYCLOCK.

NOTE

If the MPU sends a command when the keyboard is sending data, the keyboard suspends its data transmission and KEYCLOCK to "listen" to the command from the MPU. On completion of the MPU command, the keyboard continues KEYCLOCK and keyboard data transmission from the point where transmission was suspended.

RS-232 Host Interface

The receive and transmit protocol for the RS-232 host interface (Channel B) is similar to the keyboard protocol.

Note that standard RS-232 signals input to and exit from the DUART. The input signals are used by the DUART to activate interrupt signals depending on the transmit/receive activity at the host connector. For example:

The DUART receives serial data from a host on the RECDATA line. Data is clocked into the DUART at the BAUDCLK-derived rate, where it is placed in a holding register. The DUART activates the IRQ and RECINT interrupt lines to inform the GLUE logic that a byte of host data is residing in the DUART. GLUE interrupts the CPU. The CPU then reads the data by way of the IOD bus and the GLUE gate array. The CPU then activates the RDN, causing the DUART to place the data byte on the IOD data bus.

When transmitting to the host, the MPU logic checks the DUART status register. If the DUART is not busy, the TRANINT (transmit interrupt) line goes active, signifying that the DUART is ready to receive data from the IOD bus. The MPU places data on the IOD data bus, addresses the DUART, and sets WRN high. The DUART latches the IOD data and transmits it bit-serially to the host at the BAUDCLK-derived rate.

This concludes the RS-232 HOST interface protocol description.

Auxiliary Host Port. An alternative host serial port (can be used as an alternative to the keyboard or the host ports. The alternative port is available at pins 16 and 14 of J945. (Normally, these pins are not used.) Refer to Schematic 11.

The alternative port is enabled by cutting the 0-ohm resistor, W465. This pulls up the KEY DATA line inside U558, effectively disabling the KEYDATA input. At the same time, pin 16 of J945 is enabled, allowing it to receive data from an RS-232 source. Pin 14 of J945 is the RS-232 output to the alternate serial device.

COMM Pack Interface

Introduction

Communication packs provide a customized communications link between the MPU board and an external controller. COMM Packs are available for RS-232-C, GPIB, and 8-bit parallel printer protocol.

COMM Packs plug into a connector mounted directly on the MPU board. The MPU manages all COMM Pack communications.

Section 3: Connectors and Cabling, shows the connector pin/signal assignments for the COMM Pack connector, J580.

The MPU communicates with a COMM Pack, as follows. Refer to MPU Board Schematic page 4 and the Detailed MPU Board Block Diagram in the *Diagrams* section when reading the following.

Power-On and Reset

During the power-on sequence or at reset, the COMM Pack circuits are set to a known condition. IOD3 and GBA[9:11] are set high, thus keeping the PAKINT (COMM Pack Interrupt) signal inactive low via the operating characteristics of exclusive-OR gate, U370.

Interrupt Control

PAKINT is controlled as follows:

Whenever the COMM Pack needs to be serviced by the MPU, it pulls up on the COMPKIRQ (COMM Pack Interrupt Request) signal line. This causes the PAKINT signal to go high, signalling the MPU via the interrupt multiplex circuit that the COMM Pack needs its attention. The MPU addresses the COMM Pack, obtains status information, and manages the request for service, whether read data, write data, etc.

When the MPU services the COMM Pack's interrupt request, the COMM Pack pulls the COMPKINQ signal low, and the cycle repeats, as needed.

In the event a COMM Pack is removed when the MPU is powered on, COMPKIRQ goes active high via PK/. A PAKINT signal is generated signalling the MPU that the COMM Pack port needs servicing. The MPU addresses the port and discovers that the COMM Pack has been removed. With this discovery, the MPU, via the GLUE gate array, sets Glue address bits 9, 10, 11 to 0,1,0, respectively, and data bit IOD3 to 0. This causes PK/ to go active low, setting PAKINT inactive low. The MPU thus clears the interrupt condition, enabling the MPU to continue other operations. As previously mentioned, the MPU resets PK/ to a high state, thus keeping PAKINT inactive-low.

When the MPU is in a power-on condition, and a COMM Pack is inserted into the COMM Pack slot, the COMPKINT line immediately goes low. PAKINT goes active high, alerting the MPU that the COMM Pack has generated an interrupt. The MPU addresses the COMM Pack, reading its status and ID bits. Both PK/ and COMPKIRQ are set low, disabling PAKINT via the exclusive-OR action of U370.

Reading the COMM Pack's ROM

When reading the following description assume the RS-232-C COMM Pack is installed.

When the MPU board wants to read data from the COMM Pack ROM, it places the ROM data address on the BBA[1:16] address bus. BLDS/ and BUDS/ are both logic high, causing ABENABLE/ to enable the address buffer. This places address bits BBA[1:16] onto the ACPK[0:15] bus. ACPK 15 (CROM/) is low, and enables the

COMM Pack ROM. The GLUE gate array logic sets PACKREAD logic low, causing IO_READ_L to read the addressed data from the COMM Pack's ROM. This data appears on the D[0:7] bus.

IO_READ_L causes D[0:7] data to pass through the bi-directional data buffer to the BD[0:15] data bus.

Data Transmitting and Receiving

The MPU board can communicate with a COMM Pack in either byte (8-bit), or word (16-bit) format. Currently, only byte communications is used. (Sixteen-bit communication is described despite the fact that 16-bit word format is reserved for future applications.)

Byte Read From COMM Pack. Data from the COMM Pack to the MPU has three sources. Two of these sources are from within the COMM Pack; the third data source is the host connected to the COMM Pack.

One source, the COMM Pack ROM, has been discussed under the heading *Reading COMM Pack ROM*. The following describes how status and host communications data is received from the COMM Pack.

The COMM Pack status byte is sent to the MPU as follows:

Either as initiated by the MPU, or as the result of a COMM Pack request for service (COMPKIRQ going logic high), the MPU sets address bits BBA[1:3] to request the status byte from the COMM Pack. ABENABLE/ goes low active to allow the command code to pass to the ACPK[0:15] address bus. The COM_IC_SELECT signal is low-active to enable the COMM Pack communications IC (in the COMM Pack). When the GLUE gate array sets PACKREAD low, the status byte is strobed out of the COMM Pack and onto the D[0:7] data bus. COMPKIRQ may then go low. IO_READ_L will be low-active, placing the status byte onto lines 0-7 of the BD[0:7] data bus.

A read from the host occurs in much the same manner as a status byte read. The 1.81 MHz clock provides timing for the COMM Pack. When the COMM Pack has assembled a byte of data to be sent to the MPU, it pulls up on the COMPKIRQ interrupt line. The MPU responds, setting COM_IC_SELECT low-active and requests COMM Pack status. Upon determining that the COMM Pack has a byte of data to send, the MPU sets IO_READ_L low-active. COMPKIRQ is reset and the data byte is strobed from the COMM Pack, through the data buffer, and onto lines 0-7 of the BD[0:15] data bus. The cycle repeats, as needed.

Byte Write to COMM Pack. When data is to be written to the COMM Pack, COM_IC_SELECT is low-active and PACKREAD is high active. PACKREAD causes bits 0-7 on the BD[0:15] data bus to be placed on the D[0:7] data bus. PACKREAD then goes logic low, enabling IO_READ_L to strobe the data byte into the COMM Pack. The COMM Pack acknowledges receipt of the data byte by setting COMPKIRQ active high. The cycle repeats, as needed.

8/16-Bit Communications. When the MPU discovers that a COMM Pack is installed (as a result of power-on sequence or inserting COMM Pack following a power-on sequence), it checks ROM Location 0 to determine what kind of COMM Pack is installed. If, after communications with the COMM Pack, the MPU determines a 1200-style COMM Pack is installed, it sets COMM Pack communication parameters for 8-bit operation. (The ALATCH/ and SIZE_SELECT_8/16 signals are not used for 8-bit COMM Packs that can only communicate in eight-bit bytes.) And, because the MPU software talks in data byte format, only one data byte strobe (BLDS/) is active.

Should 16-bit wide COMM Pack be installed, communication between it and the MPU would generally be as follows:

NOTE

The differences between byte (8-bit) and word (16-bit) data transfer are associated primarily with COMM Pack data bus and address bus operation.

If MPU software recognizes a 16-bit COMM Pack, then the MPU sets COMM Pack communication parameters accordingly. SIZE_SELECT_8/16 selects between 8 and 16 bit communications. ALATCH/ latches the data address into the 16-bit COMM Pack.

Refer to Figure 4-18. When data is to be written from the MPU to the COMM Pack, the MPU sets both BLDS/ and BUDS/ logic low. With PACK/ and SIZE_SELECT_8/16 active-low (clocked by 10 MHz) and PACKREAD high, data is transferred 16-bits parallel from the BD[0:15] data bus to the D[0:7] and ACPK[7:14] buses. The SIZE_SELECT_8/16 and ALATCH/ signals allow the ACPK[7:14] lines to be multiplexed for bits 8-15 of a 16-bit data transfer.

When data is to be written from the COMM Pack to the MPU, the basic difference is that PACKREAD/ is logic-low to enable simultaneous transfer of 16 data bits from the D[0:7] and ACPK[7:14] buses to the BD[0:15] bus.

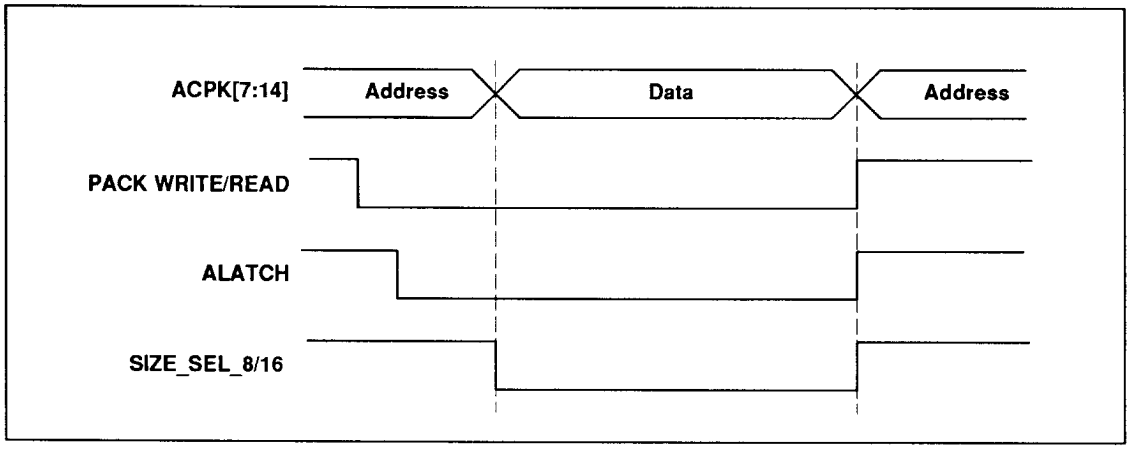


Figure 4-18. COMM Pack read/write timing.

Acquisition Module Interface (TekLink)

Introduction

Acquisition modules interface to an MPU board using TekLink, a high-speed serial data interface. TekLink is the system interface for an analyzer system. It consists of a 26-pin conductor bus used for serial data transfer between an MPU board and acquisition modules, and for synchronization of events between acquisition modules. TekLink identifies acquisition modules as being internal or external to a mainframe system. TekLink protocol facilitates system configuration, acquisition module setup, run time control, and data read-back for any connected internal and external modules.

This material describes the TekLink Interface. The following subjects are explained:

- Physical description
- Signal descriptions
- Data transactions
- Acquisition module synchronization
- Thermal sense
- TekLink timing
- TekLink circuits

Physical Description

Separate but functionally identical links are provided for internal and external acquisition modules. Internal acquisition modules reside in a mainframe that contains an MPU board. External modules reside in expansion mainframes and connect to an MPU using an external TekLink connector and cabling.

The minimum TekLink configuration consists of a host and one internal acquisition module. Other configurations (see Figure 4-19) consist of up to two internal acquisition modules, and up to two external acquisition modules residing in an expansion mainframes. The following describes the internal and external TekLink connections.

Internal Module TekLink Connect. Internal acquisition modules attach to an MPU board using a 26-conductor ribbon cable. This same method is used to connect acquisition modules inside an expansion mainframe.

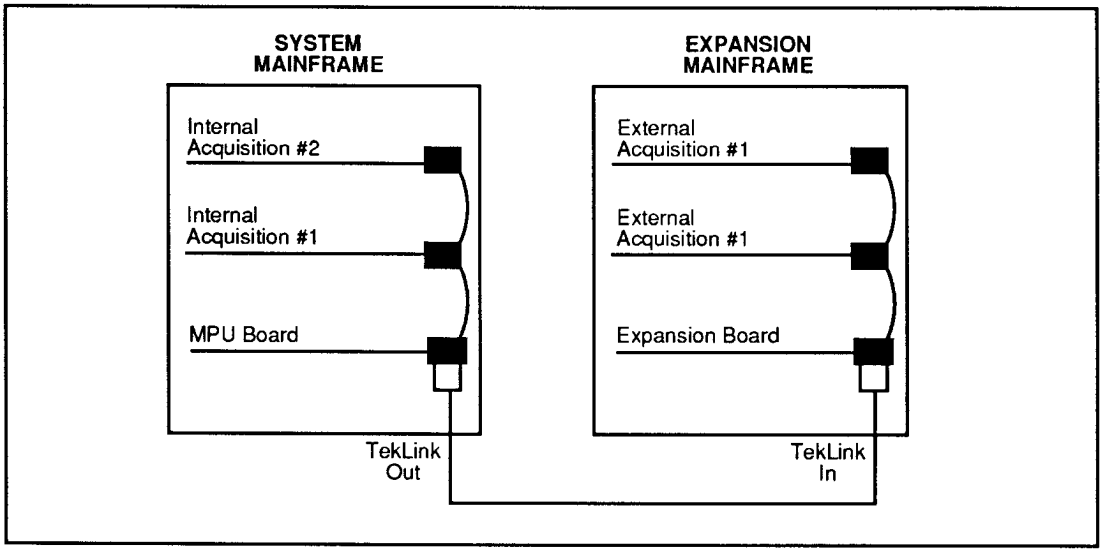


Figure 4-19. TekLink interconnect block diagram.

External Module TekLink Connection. See Figure 4-19. The MPU board can connect to an Expansion Mainframe via the external TekLink cable. The MPU board has an external TekLink connector for this purpose. The TekLink cable mates to the TekLink Connector on the Expansion board in an Expansion Mainframe. Signal termination is provided on the Expansion board.

NOTE

The external TekLink signals are functionally identical to the internal TekLink signals. Refer to TekLink Circuit Descriptions later in this section for explanation of signal source.

Signal Description

The following is a general description of the TekLink signals. Some signals are followed by an "X". The "X" indicates signals used by both internal and external acquisition modules, but which originate from different sources on the MPU board.

SIGNAL [1:4]. These general purpose signals are used between acquisition modules to facilitate recognition of trigger occurrences. Signals are active-high, wire-ANDed, and are synchronous with either SCLK, or with MCLK qualified with SCLK.

SYS_TRIG~. This is the system trigger. It is a special purpose event line driven by modules to correlate the occurrence of a user-defined system trigger condition. High = armed; high-to-low transition = trigger; held low = hold-off. SYS_TRIG~ is wire-ORed between modules; and is synchronous with either SCLK, or with MCLK qualified with SCLK.

RUN. This is the run(stop) control signal from the MPU to start and stop an active acquisition window for time base correlation. High = run; synchronous with either SCLK, or with MCLK qualified with SCLK.

MCLKX. The 50 MHz master clock, differential ECL (+5 V) reference for all TekLink transactions. It is sourced from the MPU.

SDX. A bi-directional serial data line used to transfer 16-bit address and data words between acquisition modules and the MPU.

SCLKX. The 12.5 MHz serial data clock used for synchronous transmission of serial data, handshake, and events. It is an AC CMOS signal derived by dividing MCLK by 4.

HSX. A bi-directional, serial-control data handshake line for shifting time-multiplexed request/grant "frames" between host and modules.

NOTE

The MPU has separate handshake lines: HS for internal handshake and HSX for external handshake.

DIRX. The direction signal from the MPU indicating direction of HS request/grant data. For an example, refer to Figure 4-20. (See also *Handshake Timing.*) When DIR is low, the first eight "frame bit times" of a 16-bit handshake frame are shifted from the acquisition modules to the MPU with each rising edge of SCLK. When DIR is high, grants (the last 16 bits of the handshake frame) are shifted from the MPU to acquisition modules.

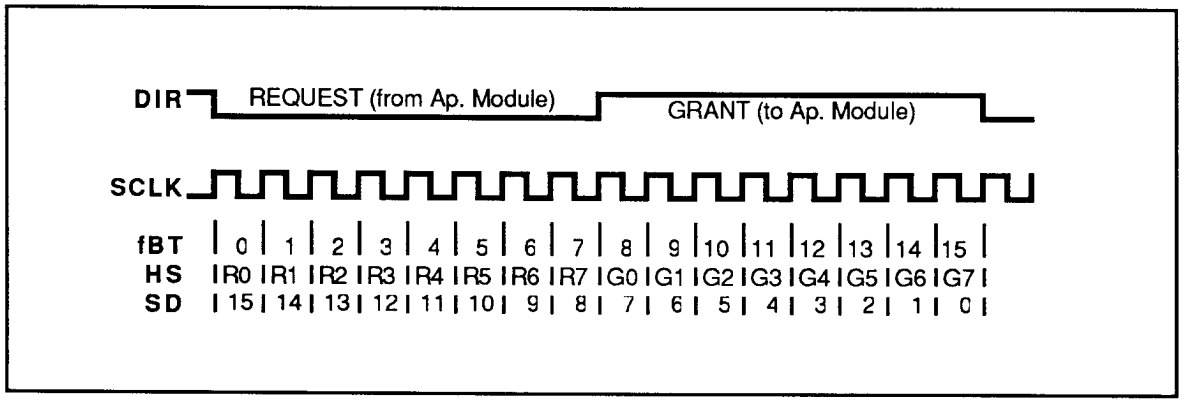


Figure 4-20. DIR control of request/grant data frame.

NOTE

All modules sample grant status during FBT 0 and the MPU samples request status during FBT 8.

The DIR (internal TekLink) and DIRX (external TekLink) signals are functionally identical but are individually buffered.

The purpose and function of TekLink signals are thoroughly explained in the following descriptions.

Data Transfer Transactions

There are three modes of data exchange: immediate (read/write), block transfer (read/write), and interrupt. With each communication mode, data is transmitted serially in 16-bit words (frames) relative to both the 12.5 MHz serial data clock (SCLK) and a request/grant handshake protocol. All three communication modes share a common request/grant asynchronous handshake protocol.

Immediate Mode. Immediate mode is used for very short data transfers; e.g., register set-up, programming small non-sequential segments of memory, etc.

An immediate mode transfer is indicated when an acquisition module receives a grant without having a currently outstanding interrupt request (see *Handshake* below). An immediate exchange consists of two successive frames: a command address frame and a data transfer frame. The command address frame is from the MPU to the acquisition module. It signifies a read or write function (read = 1). The 16-bit data transfer (read or write) frame (B-E through B-0) is acquisition module specific, i.e., address space depends on design of specific acquisition module.

NOTE

On an immediate read, the first serial data bit from the acquisition module is clocked out using the same rising edge of SCLK used to clock in command address B0. Therefore, in order to have time to prepare data for transfer, the last few command address bits are not used.

Block Transfer Mode. Block transfer mode is used to transfer large amounts of data. The MPU initiates a block transfer (with two immediate writes) by first resetting the acquisition module's address counter and then issuing a block transfer enable command, i.e., turning on the acquisition module's block enable bit. With its block enable bit set, the module continues to issue requests and either log in or transfer data with corresponding grants from the MPU. This process continues until a time-out. A time-out is defined as a minimum of eight consecutive requests from an acquisition module for which it receives no grant from the MPU.

The MPU TekLink interface circuitry has two 4 Kbyte transfer buffers. It can multiplex two concurrent block transfers to two different acquisition modules simultaneously. The TekLink interface controls the length of the transfer. The acquisition module keeps track of its current data transaction by incrementing its address counter.

Interrupt Mode. Interrupt mode allows acquisition modules to assert a request for service. A pending request remains active until serviced by the host via a grant. On receipt of a grant, the acquisition module returns one word and clears its interrupt enable bit.

NOTE

Interrupt mode and block transfer mode are mutually exclusive; i.e., before block transfer is enabled, interrupts are disabled so the acquisition module is able to determine the receipt of a grant.

Handshake Protocol. A request/grant asynchronous handshake protocol is common to all three data transaction (communication) modes.

Handshake consists of the bi-directional serial shift of data on the serial data (SD) line. Initially, eight bits (a request) are shifted from the daisy-chained acquisition modules to the MPU; then eight bits (a grant) are shifted from the MPU to the acquisition modules.

NOTE

There are separate HS (handshake) signal lines for internal and external modules.

At the instant in time when all eight bits have been shifted out from the MPU, any, or all acquisition modules may assert a request by setting the FBT (frame bit time). The eight request bits are then shifted back to the MPU for interrogation. The MPU responds with a grant by re-asserting the FBT of the corresponding acquisition module and shifting the handshake word back to the acquisition modules.

Requests are shifted in as FBT-0 through FBT-7; grants are shifted out as FBT-8 through FBT-F. On FBT-F, each acquisition module checks to see if it has received a grant. If a module detects a grant but has no outstanding request, an immediate mode (unsolicited) transaction occurs. If the module has an outstanding request, the grant is the response to either an interrupt request or a block request. Transactions occur accordingly. If no grants are detected, an idle state is implied. If a module asserts a request and receives no grant for at least eight consecutive frames, the module will "time out."

Acquisition Module Synchronization

TekLink facilitates synchronization of events between acquisition modules using four SIGNAL lines, the RUN(stop) line, and the SYS_TRIG~ (system trigger) line. All system run-time activities on these lines are synchronized with the 50 MHz master clock (MCLK) and the 12.5 MHz serial data clock (SCLK). (SCLK is derived from MCLK and therefore maintains continuous phase synchronization.)

SIGNAL Lines. The four SIGNAL (SIGNAL[1:4]) lines are open collector, wire-ANDed, true high signals. Any acquisition module may drive and/or monitor these lines. If a module is not programmed to participate on the SIGNAL event lines, its drivers will have been instructed to float high. Modules which participate in determining trigger conditions must maintain the appropriate SIGNAL event line low until their specific condition has been satisfied, after which it can drive the line high.

RUN. The RUN signal line is driven by the MPU to define an active acquisition window across all acquisition modules, except those which have been programmed to the OFF state. (An OFF state module will not participate in an acquisition or display.) RUN is activated relative to a user's START/STOP key. The acquisition is stopped by a re-acquisition of the START/STOP key or by MPU recognition of module done status (this is done using run-time polling).

System Trigger. The system trigger (SYS_TRIG~) line is a wire-ORed signal, driven by acquisition modules. It is used to synchronize acquisition events among acquisition modules.

There are two types of user-programmable triggers: (1) module trigger and (2) system trigger. Only a system trigger causes modules to assert the SYS_TRIG~ signal line.

NOTE

A trigger signal at the MPU external TRIG IN port is treated as a system trigger.

System triggers always have precedence over module triggers. Consequently, occurrence of a system trigger causes all modules to trigger, regardless the status of individual module triggers.

NOTE

If a module is in "not off state," and is not programmed to participate in a system trigger event, it must be instructed to float its TekEvent trigger driver high.

Refer to Figure 4-21.

When RUN is initially asserted at the beginning of an acquisition cycle, the SYS_TRIG~ line may be in either an armed state (high) or a hold-off state (low). (Hold-off implies that one or more modules need a pre-fill period prior to a trigger-arm state.) When the last module satisfies its requirements, it allows the SYS_TRIG~ line to go to the arm state (high). Any module which has been programmed to participate in a system trigger SIGNAL event, may subsequently assert the SYS_TRIG~ line (low) when its trigger conditions are satisfied.

Following a high-to-low transition of the SYS_TRIG~ signal, all modules will hold the SYS_TRIG~ line in the hold-off state until their post-fill (and possible subsequent pre-fill) conditions are satisfied. The last module to satisfy its requirements allows the SYS_TRIG~ line to again return to the arm (high) state.

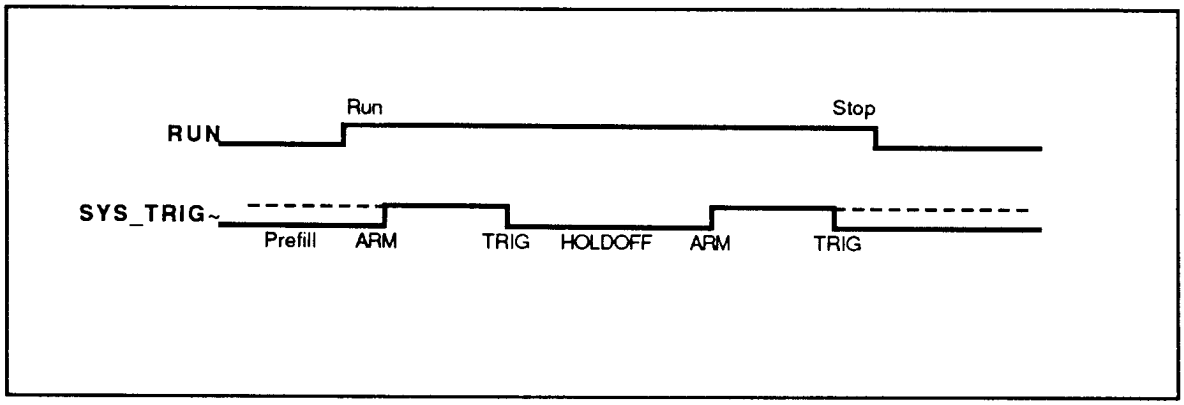


Figure 4-21. Typical system trigger functions during a RUN cycle.

As shown in Figure 4-21, there may be more than one SYS_TRIG~ within a single RUN cycle. This occurs to facilitate filling of partitioned memories. These memory partitions may be filled by either a module's trigger or by a system trigger. For example, if a module has partitioned memory and a system trigger occurs, only the "current" memory partition is filled. (Current partition is defined as the next available partition in a sequence of partitions.) The module will also participate in trigger hold-off. The remaining (subsequent) partitions will fill relative to their user-programmed trigger conditions for a module and/or system triggers. Finally, via continuous status polling, the MPU detects and terminates the RUN cycle.

Throughout a RUN cycle, the MPU constantly polls acquisition modules to determine status. When all modules indicate "done," i.e., no pending module or system triggers, the MPU signals STOP to all modules by lowering the RUN signal line. If a user terminates a run cycle using a system START/STOP key (hardware), the display trigger indicator (on system display device) will be positioned at stop, but only if no triggers have occurred. If the run cycle terminates as the result of all trigger conditions being satisfied, the most recent trigger (whether a module or system trigger) is used as the display trigger indicator.

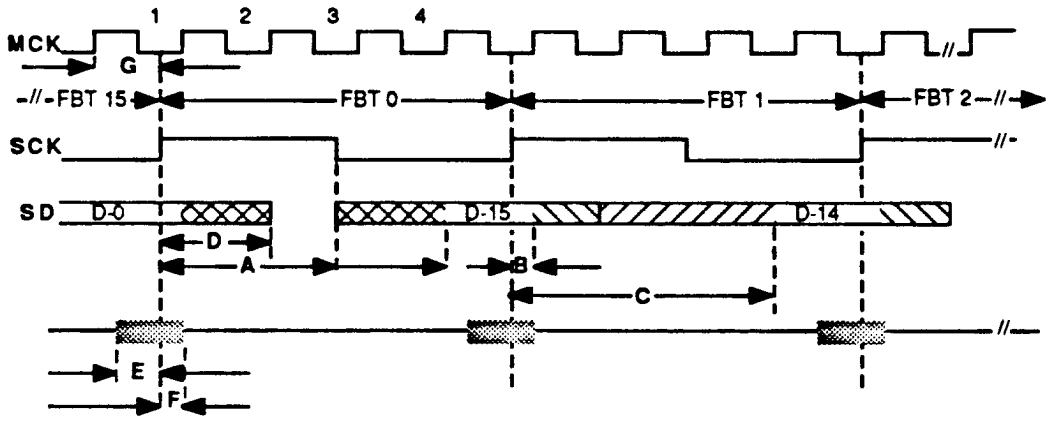
Thermal Sense

The thermal sense line (THERM) provides the capability for an acquisition module to cause total system power shut-down if a module detects an over-temperature condition. All acquisition modules are wire-ORed to this line. Should an acquisition module experience a thermal problem, a thermal switch (mounted on the acquisition module) pulls this line to ground. When the MPU detects less than 500 ohms to ground on the THERM line (asserted by any module), an SCR in the MPU board's power control circuit shuts down the mainframe's power supply. When the thermal switch opens, power will be restored. Refer to *Section 8: Troubleshooting,* for additional information regarding this signal line.

TekLink Timing

The following serial data and handshake timing specifications are referenced to the TekLink connector at the acquisition modules.

Serial Data Timing. Refer to Figure 4-22 and 4-23. Data is transmitted to and received from acquisition modules in 16-bit data words on the bi-directional SD signal line. Data is synchronous and is clocked with either SCLK, or with the first phase of MCLK. Data exchange between the MPU and an acquisition module occurs on FBT 0 when the active module tri-states and the next authorized device module enables its tri-state drivers. Note that the MPU enables its tri-state drivers with the falling edge of SCLK during FBT 0.



HOST WRITE DELAY (Delay is in Nanoseconds)

A. Tri-state to Data = 40 min. to 65 max.
B. Next SCK to Data Invalid = 5 min.
C. Next Data Valid = 65 max. (Typical = 25)
D. Data to Tri-State = 25 max.

MODULE READ (Set-up/Hold)

E. Set-up = 10 max.
F. Hold = 5 min.
G. MCK to SCK = 9+/-6 (MCK = 50 MHz; SCK= MCK ÷ 4)

Figure 4-22. MPU write/module read timing.

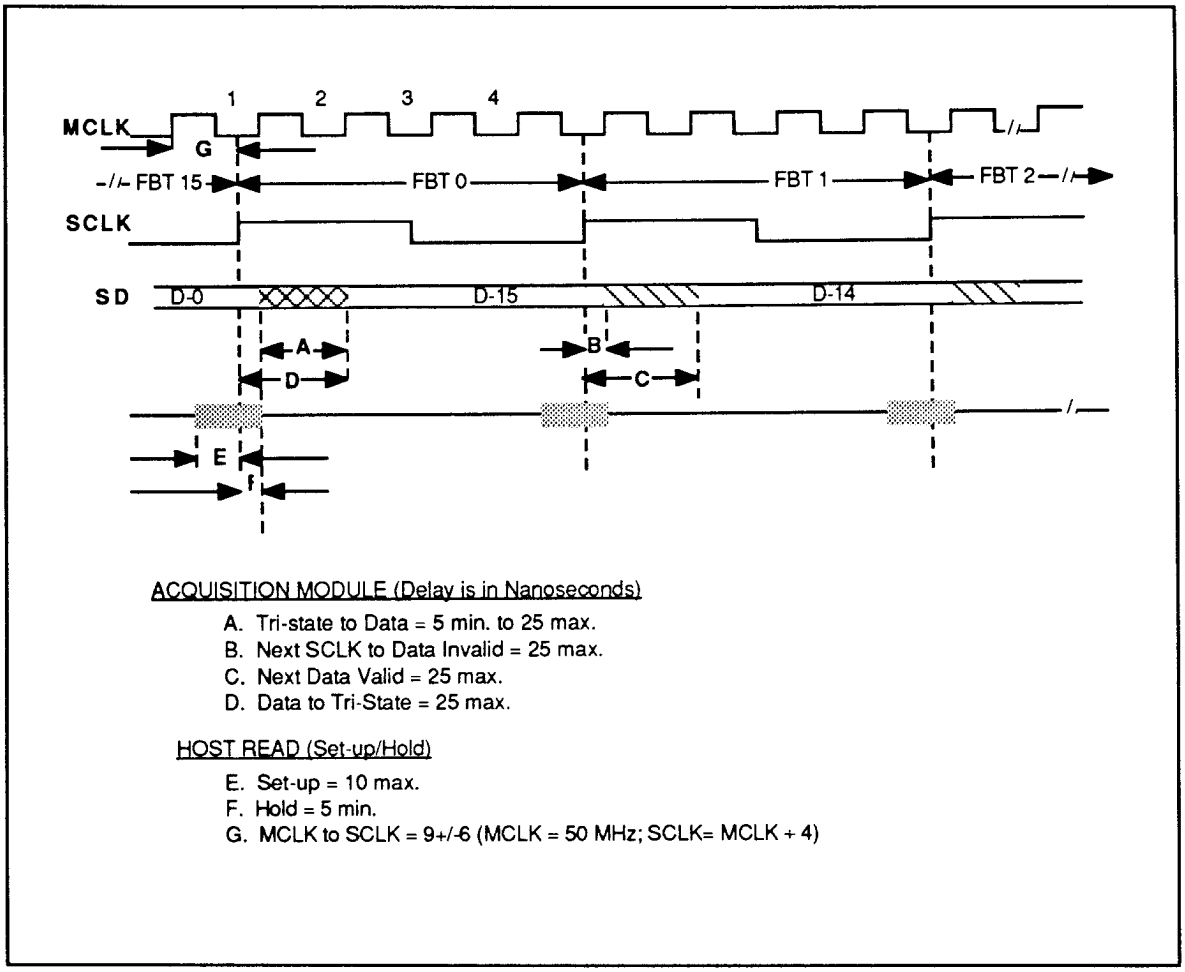
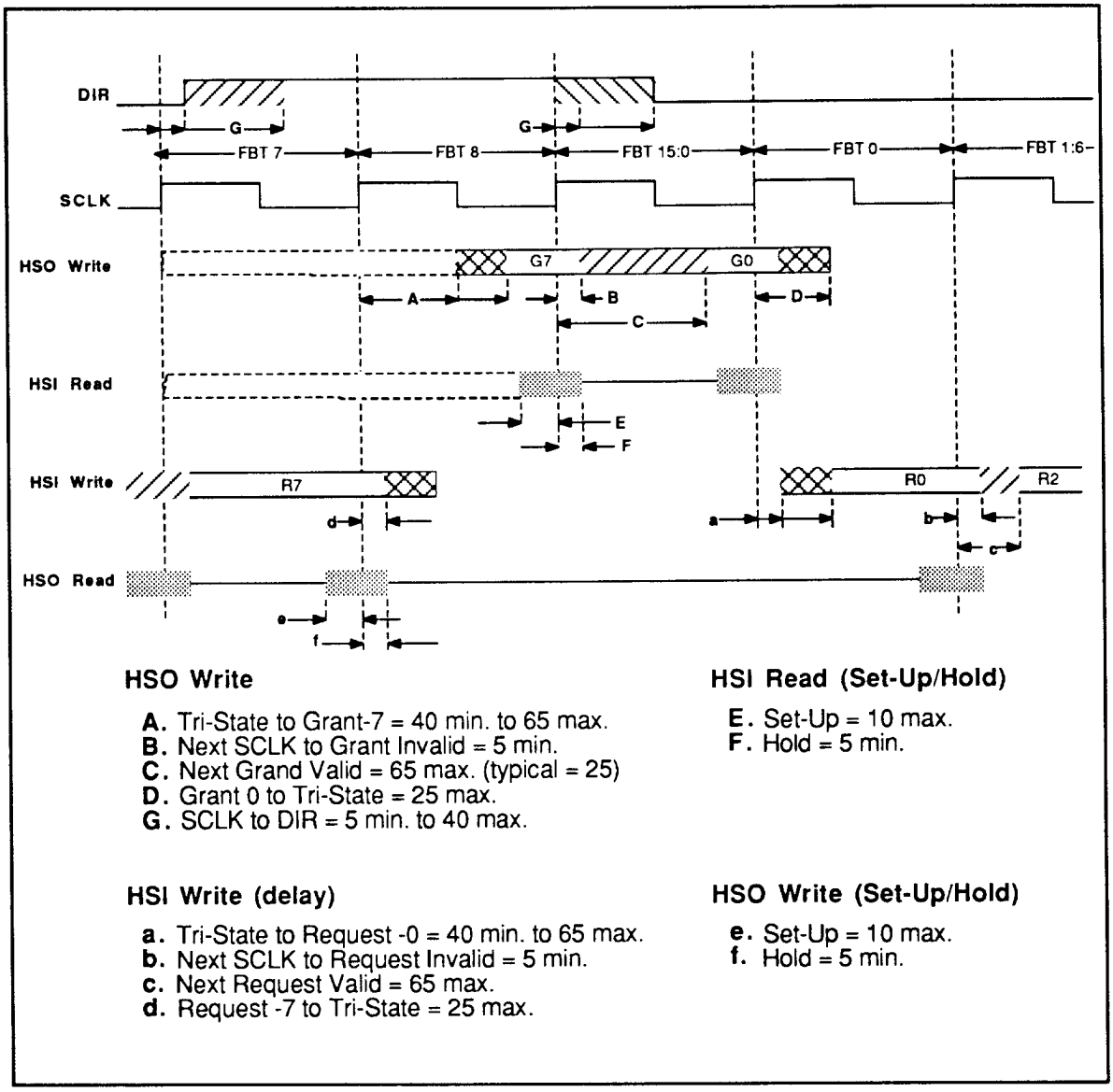


Figure 4-23. Application module write/MPU read timing.

Handshake Timing. Two handshake timing diagrams are provided. Figure 4-24, shows the timing characteristics of the HS signal line. Figure 4-25 shows the timing relationships of the SIGNAL[1:4], SYS_TRIG~ and RUN signals lines in relation to MCLK and SCLK.



HSO Write

A. Tri-State to Grant-7 = 40 min. to 65 max.
B. Next SCLK to Grant Invalid = 5 min.
C. Next Grand Valid = 65 max. (typical = 25)
D. Grant 0 to Tri-State = 25 max.
G. SCLK to DIR = 5 min. to 40 max.

HSI Read (Set-Up/Hold)

E. Set-Up = 10 max.
F. Hold = 5 min.

HSI Write (delay)

a. Tri-State to Request -0 = 40 min. to 65 max.
b. Next SCLK to Request Invalid = 5 min.
c. Next Request Valid = 65 max.
d. Request -7 to Tri-State = 25 max.

HSO Write (Set-Up/Hold)

e. Set-Up = 10 max.
f. Hold = 5 min.

Figure 4-24. Handshake timing.

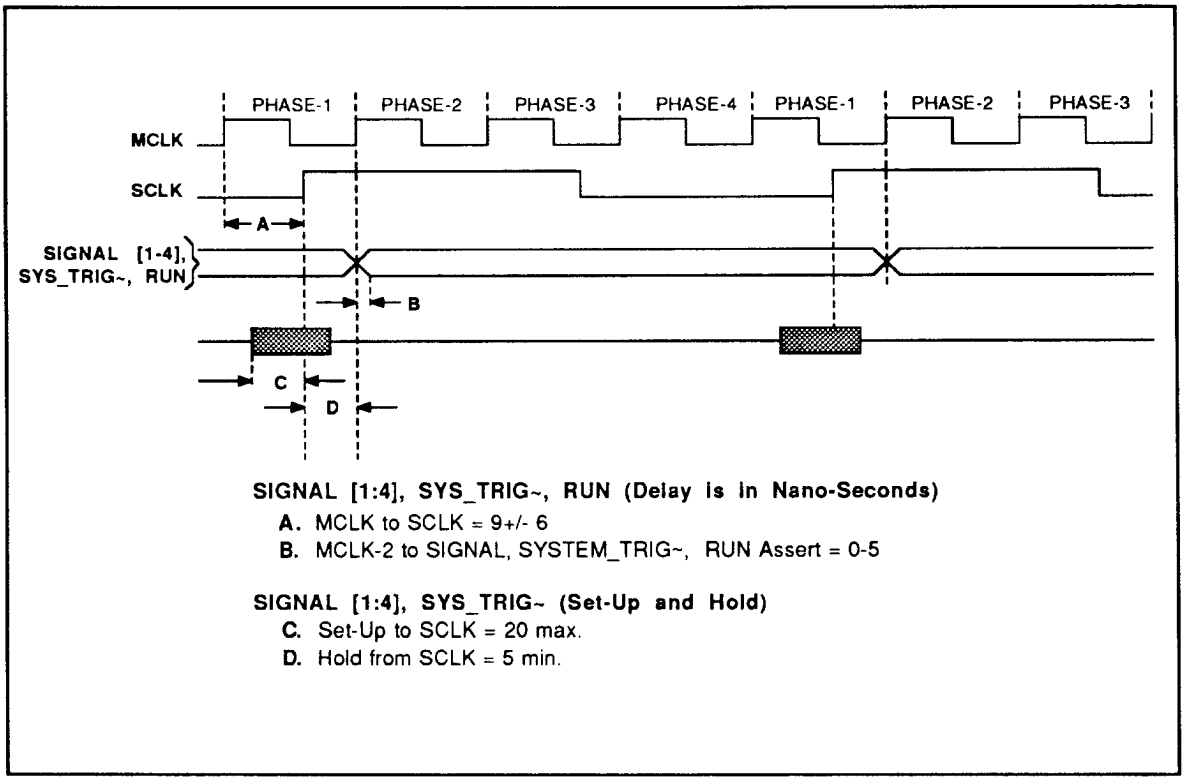


Figure 4-25. SIGNAL, SYS_TRIG/, and RUN timing.

SIGNAL[1:4], SYS_TRIG/, and RUN signal lines are synchronously asserted relative to the rising edge of MCLK phase 2 or the rising edge of SCLK. SIGNAL[1:4], SYS_TRIG/ and RUN signal lines are sampled relative to the rising edge of SCLK or the rising edge of MCLK phase 1.

Circuit Descriptions

Refer to Figure 4-26. The TekLink Interface is comprised of the following circuits:

- TekLink gate array
- TekLink RAM
- TekLink clock
- SIGNAL line buffers
- External trigger and level shift
- Trigger and Run delay

Read the preceding signal and protocol descriptions before reading the following circuit descriptions. Refer to MPU Board Schematics 15-19, and the MPU Board Detailed Block Diagram in *Section 11: Diagrams* when reading the following.

TekLink Gate Array. This 120-pin gate array (U720) functions as the controller between the MPU data/address buses and the acquisition modules connected to the TekLink interface. It manages all communications protocol. For additional information about TekLink Protocol refer to the preceding *Data Transfer Transactions* description. *Section 3: Connectors and Cabling* contains an illustration that shows the pin/signal assignments for the TekLink gate array.

TekLink RAM. Refer to MPU board Schematic 18 in *Section 11: Diagrams*. TekLink memory consists of two 8K X 8 (64 Kbit) RAM ICs. This memory is primarily used for temporary storage of data to/from an acquisition module.

TekLink Clock. Refer to MPU Board Schematic 16. The TekLink clock develops the MCLK and SCLK clocks from a 100 MHz oscillator and clock divider circuits.

+3 VDC Power Supply. Refer to MPU board Schematic 16. A +3 V supply is developed from +5 V by 3 V regulator LM337. This voltage is used by the oscillator and U605. U605 is used to establish ECL thresholds for selected TekLink comparator circuits.

U610 provides a 50 MHz clock for MCLK and a 12.5 MHz clock for SCLK. Both MCLK and SCLK are clocked on the rising edge of the 100 MHz clock.

Functionally, the MCLK and MCLKX signals are identical; the MCLK and MCLK/ signals are routed to internal modules and the MCLKX and MCLKX/ signals are routed to external modules. The same is true for the SCLK signals.

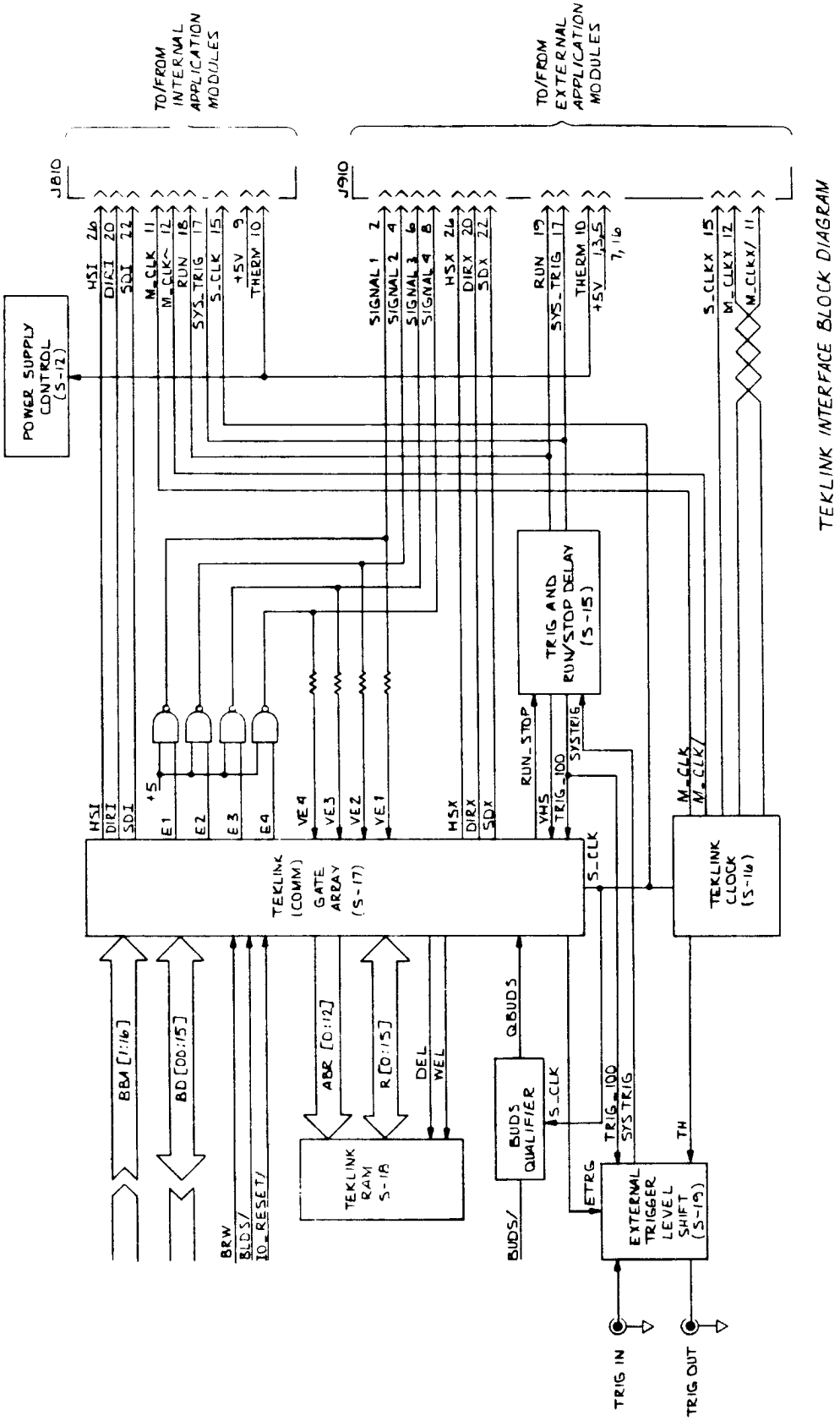


Figure 4-26. TekLink interface block diagram.

SIGNAL[1:4] Line Buffers. The signal line buffer (U713) protects the TekLink gate array from any catastrophic failure on a SIGNAL[1:4] line. The VE1-VE4 signals are exercised by diagnostic software to test the TekLink Gate array and associated circuits.

External Trigger and Level Shift. Refer to MPU Board Schematic 19. This circuit accepts TTL-level signals from the TRIG IN BNC connector and converts them to buffered ECL-level SYS_TRIG~ signals. The SYS_TRIG~ signal then triggers, or enables, an MPU board/mainframe system. It also accepts an ECL-level system trigger and converts it to a TTL-level signal, presenting it at the TRIG OUT BNC connector. This circuit functions as follows:

Transistor Q850B is a non-inverting buffer/amplifier for the TRIG IN signal to pin 10 of U753B. R753 is used to adjust the "0" (OFFSET) point at pin 10 of U753B. (Q850A provides a constant current source for the high impedance input.)

If a X1 probe is connected to J860, the TRIG IN signal level at pin 10 of U753B is 1.4 V. If a X10 probe is used, the signal level is 0.14 V. A comparator circuit (consisting of U753A and voltage divider R756, R758, and R759) provides appropriate comparison voltage at pin 9 of U753A to enable a low-going output from U753A. (If a X10 attenuation trigger input probe is used at J860, the probe connector contacts the outer ring of the TRIG IN BNC. This causes the comparator circuit to reduce the voltage at pin 9 of U753 to 0.14 V.) The low-going output from U753A is inverted by U655A, causing the SYSTRIG signal line to go high-active.

The SYSTRIG signal can also be exercised by diagnostic software. This occurs when system diagnostic routines cause the TekLink gate array to set the ETRG (external trigger) signal low-active.

SYSTRIG enters the trigger and run delay circuit, where the SYS_TRIG~ signal to the acquisition modules is delayed two SCLK clock times.

The external trigger and level shift circuit accepts an ECL-level TRIG_100 signal from trig and run delay circuit. This ECL-level signal is converted to a TTL-level signal and made available at the J950, TRIG OUT connector. This signal is useful in triggering or enabling other external instruments.

Trig and Run Delay. Refer to MPU Board Schematic 15. This circuit consists of two count-down registers. One counter provides delays for the SYS_TRIG~ and TRIG_100 signals; the other counter delays the RUN signal.

Upon receipt of a SYSTRIG signal from the external trigger circuit, the TRIG delay register delays the SYS_TRIG~ signal two SCLK times. The TRIG_100 signal is delayed three SCLK times.

Upon receipt of a RUN_STOP signal from the TekLink gate array, the RUN delay register delays the RUN signal two SCLK times. The VRS signal is delayed three SCLK times.

Section 5
VERIFICATION AND ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains three parts: *Functional Check Procedures, Performance Verification Procedures,* and *Adjustment Procedures.* This information enables a qualified service technician to verify MPU board operation and to perform adjustments.

NOTE

The verification procedures in this manual do not verify the performance of an application module. Refer to the appropriate service manual for procedures to verify each application module.

The following provides a brief definition for each type of procedure:

- **Functional Check Procedure**. These procedures may be used as an incoming inspection to verify that the MPU board is functioning properly within a Mainframe system.
- **Performance Verification Procedures**. These procedures provide a detailed check of the product specifications. Specifications listed in the performance requirements column of *Section 2: Specifications* can be verified using these procedures. Under normal circumstances, the Functional Checks within these Performance Verification Procedures provide an adequate test of product performance.
- **Adjustment Procedures.** These procedures describe how to adjust the MPU board to meet specifications. If the MPU board cannot be adjusted to meet specifications, then repair is necessary.

REQUIRED TEST EQUIPMENT

Table 5-1 lists the test equipment required to perform the procedures listed in this section. Specifications given for the test equipment are the minimum necessary for accurate verification and adjustment of the MPU board. All test equipment must be accurately calibrated and operating within the given specifications. If equipment is substituted, it must meet or exceed the specifications of the recommended equipment. Common hand tools used in these procedures are not listed.

Table 5-1
Required Test Equipment

Equipment	Specification	Equivalent Instrument
Oscilloscope, 2 channel	350 MHz bandwidth	Tektronix 2467B
Probes, oscilloscope (2 ea)	10X, 350 MHz, 1.3 m long	Tektronix P6136
Digital multimeter	$4\frac{1}{2}$ digits, 0.1% DC accuracy	Tektronix DM 504A or equivalent
Pulse generator	250 MHz	Tektronix PG 502
Frequency counter/timer	350 MHz, 1 part in 10^6 accuracy	Tektronix 2467B w/Option 06 or 09*
Power module mainframe		Tektronix TM 502A or TM 5006A
RS-232C Test Adapter		Tektronix part number 013-0173-01 (RS-232C Loop-Back Connector)
Coaxial cable, 50 Ω, with BNC connectors	RG-58	Tektronix part number 012-0208-00
System diagnostic disk		Tektronix part number 063-0165-XX (PRISM 3001 or 3002) 062-9925-XX (2505 or 2510 TestLab)

**You may use the Tektronix DC 5010 Universal Counter/Timer and P6125 Probe instead.*

OPERATING A MAINFRAME IN THE SERVICE POSITION

As stated earlier, the MPU board and one or two application modules will usually be installed in a mainframe. In most cases, you must place these boards in a "servicing position" to perform troubleshooting and servicing functions. Refer to *Placement of Modules for Troubleshooting* in *Section 6: Disassembly/Assembly* of the applicable mainframe service manual for instructions on how to place these modules in a service position.

WARNING

Cooling fan blades are not completely shielded. Therefore, after removing the mainframe top cover or cabinet, guard against injury by keeping fingers and loose objects away from the moving blades when operating the instrument in the service position.

CAUTION

When operating a mainframe with the cover removed, the fan(s) cannot provide adequate cooling for any application module(s). To provide adequate cooling, use an external fan or fans to blow air across the MPU board and the application module(s).

FUNCTIONAL CHECK PROCEDURES

All Systems

A functional check of the MPU board and connected modules can be easily done by exercising the System Diagnostic Software routines. These test routines are contained on the System Diagnostics Floppy disk. Refer to Section 9 for instructions that explain how to exercise diagnostic software.

Table 9-1 (refer to Section 9) lists test routines for the MPU board, hard disk drive, and COMM Pack modules. You can exercise these routines as part of a functional check or incoming inspection procedure. The diagnostic software floppy disk contains all the routines needed to verify operation of your system including the MPU board, hard disk drive, COMM Pack modules, and application modules. The software only loads the diagnostics for the modules included in your system.

NOTE

Verification procedures and diagnostic routines for installed acquisition modules are described in separate acquisition module service manuals.

In addition to the functional checks provided by exercising the routines listed in Table 9-1, MPU board boot code automatically verifies critical circuitry in the microprocessor kernel each time system power is cycled or the system is reset. No operator intervention is needed. Kernel tests exercised are:

- ROM verification test
- ROM checksum test
- RAM verification test
- Floppy interrupt circuit test
- Floppy and Hard Drive Verification Tests

The operating system will not boot if an error is detected in any of the above kernel tests. Refer to *Kernel Diagnostic Tests* in *Section 8: Troubleshooting* for a detailed description of these tests.

PERFORMANCE VERIFICATION PROCEDURES

Introduction

Performance verification procedures check specifications listed in the performance requirements column of Table 2-2. (Items listed in the performance requirements columns are specifications that the MPU board must meet.) If verification of the listed electrical specifications is required for incoming inspection or other purposes, perform the appropriate procedures outlined herein, as well as the MPU board adjustments described later in this section. The successful completion of the following procedures and tests will verify the performance of an MPU board:

- Functional Check Procedures
- MPU Board Clock Frequency and Trigger Tests

Functional Check Procedures

Perform the Functional Check Procedures as previously stated. After all functional checks have been performed, then continue the performance verification procedures by performing the MPU Board Clock Frequency and Trigger tests.

MPU Board Clock Frequency and Trigger Tests

Perform the following clock frequency tests to ensure that the MPU board can function as specified. If any of the following clocks do not meet performance specifications, replacement or repair of the MPU board may be required.

- Processor Clock Test
- TekLink Clock Tests
- External Trigger In and Out Test

NOTE

In any of the following checks that require a period measurement with ± 0.1% accuracy or better, you need to use a frequency counter/timer. You can use either the 2467B Oscilloscope with Option 06 or 09 (Counter/Timer) or the DC 5010 Universal Counter/Timer. Refer to the appropriate manual for instructions on how to use the instrument for measuring frequency and period.

See Figure 5-1 for test point (probe connection) locations when performing the following verification procedures.

Processor Clock Test

The 68010 microprocessor receives a 10 MHz clock signal from the GLUE gate array. A master oscillator inputs a 40 MHz clock signal to the GLUE gate array that divides the frequency, using internal circuits, to generate several system clocks. The 10 MHz processor clock is the critical clock signal for processor timing. If the 10 MHz clock does not meet specification, then suspect the 40 MHz oscillator or the GLUE gate array IC. Perform the following to check the 10 MHz clock:

1. Set oscilloscope controls as follows:

Input Sensitivity	1 V/division
Input Coupling	DC
Display Mode	CH 1
Timebase	20 ns/division
Trigger Mode	NORMAL
	INT (Internal)
	DC Coupling
Trigger Source	CH 1
Trigger Slope	+ (Positive)

2. Connect the channel 1 probe to pin 55 of U518 (see Figure 5-1 for location).
3. Check that the 10 MHz Clock frequency meets the specification listed on page 2–3 and that the duty cycle is 50%.
4. Disconnect the probe from the MPU board.

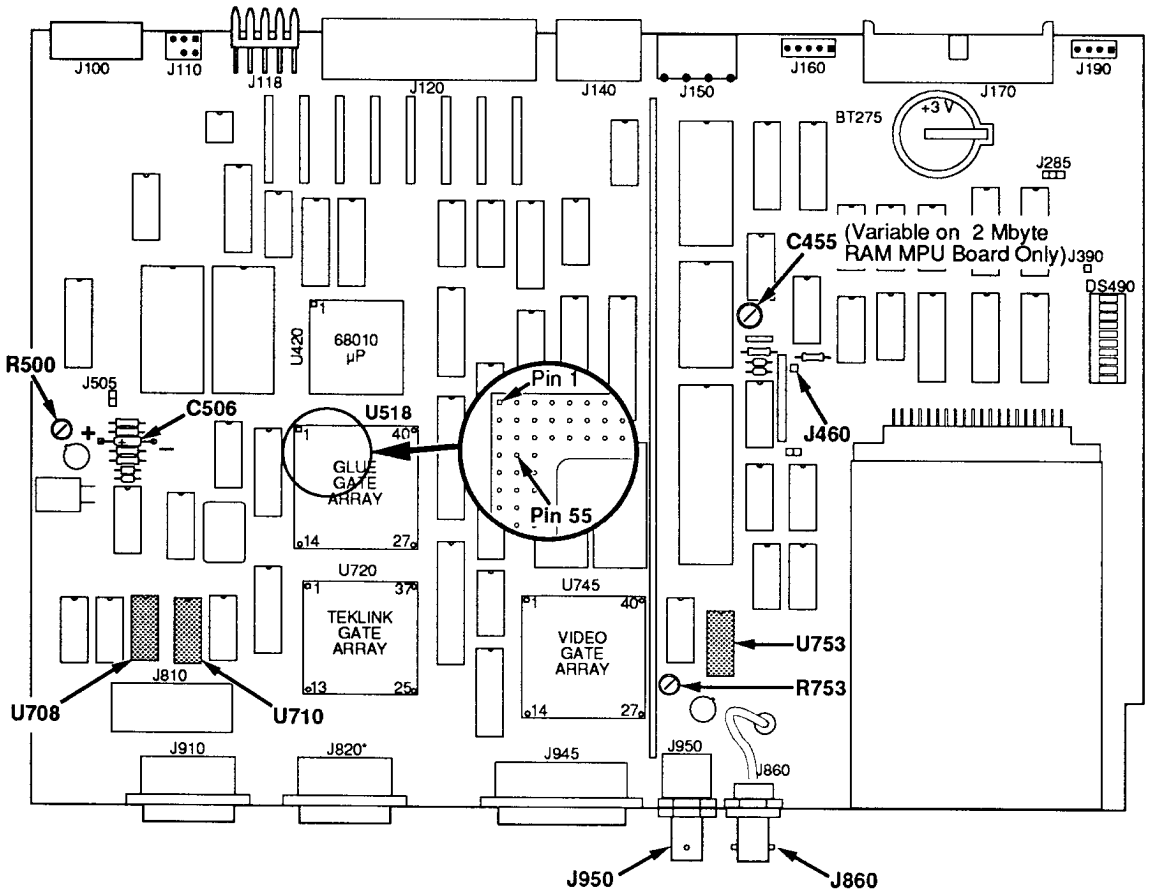


Figure 5-1. MPU board test point and adjustment locations.

MCLK TekLink Clock Test

The TekLink Interface uses several master clocks to control timing between the MPU board and the application module(s). These clocks are M_CLK and S_CLK. Both clocks are derived from the 100 MHz master clock frequency. Use the following procedures to verify the M_CLK clock frequency and duty cycle:

1. Set oscilloscope controls as follows:

Input Sensitivity	500 mV/division
Input Coupling	DC
Display Mode	CH 1
Timebase	5 ns/division
Trigger Mode	NORMAL
	INT (Internal)
	AC Coupling
Trigger Source	CH 1
Trigger Slope	+ (Positive)

2. Connect the channel 1 probe to pin 2 of U710 (see Figure 5-1 for IC location).

3. Check that the M_CLK/ clock period is 20 ns (50 MHz) ± 0.005% with a 50% duty cycle.
4. Repeats Steps 2 and 3 for the other clock signals, M_CLK, M_CLKX, and M_CLKX/, at pins 3, 14, and 15 of U710, respectively.
5. Disconnect the probe from the MPU board.

SCLK TekLink Clock Test

Use the following procedures to verify the S_CLK clock frequency and duty cycle:

1. Set oscilloscope controls as follows:

Input Sensitivity	2 V/division
Input Coupling	DC
Display Mode	CH 1
Timebase	10 ns/division
Trigger Mode	NORM
	INT (Internal)
	AC Coupling
Trigger Source	CH 1
Trigger Slope	+ (Positive)

2. Connect the channel 1 probe to pin 9 of U708.
3. Check that S_CLK clock period at pin 9 is 80 ns (12.5 MHz) ± 0.005% with a 50% duty cycle.
4. Disconnect the probe from the MPU board.

External Trigger In/Out Test

This procedure verifies the functioning of the External Trigger In and External Trigger Out circuits. Proceed as follows:

1. Set oscilloscope controls as follows:

Input Sensitivity	10 V/division
Input Coupling	DC
Display Mode	CH 2
Timebase	1 ms/division
Trigger Mode	AUTO
	INT (Internal)
	DC Coupling
Trigger Source	CH 2
Trigger Slope	+ (Positive)

2. Set PG 502 Pulse Generator controls as follows:

Back Term	push switch in
Norm In/Out	set to + position
Variable Pulse Duration	turn all the way CCW
Variable Period	turn all the way CCW

2. Connect a 3-foot, 50Ω coaxial cable from the output of PG502 to channel 1 of the oscilloscope.
3. Using the high and low output voltage knobs, adjust the PG 502 Signal Outt for a 1 kHz, 4 V_{p-p} signal with a low of 0 volts and a high of 4 volts.
4. Disconnect the PG502 output from the oscilloscope and connect it to the EXT TRIGGER IN connector, J860, on the MPU board.
5. Connect a 50 Ω coaxial cable from EXT TRIGGER OUT connector, J950, on MPU board to the channel 1 input of the oscilloscope.
6. Check that the External Trigger Out signal is about 4 V_{p-p} with a 1 kHz frequency.
7. Check the X10 probe circuit on the MPU board as follows:
   a. Disconnect oscilloscope from MPU board.
   b. Change the channel 1 volts/division setting of oscilloscope to 100 mV/division.
   c. Reconnect the PG502 to channel 1 of the oscilloscope and adjust the output of the PG502 for a 400 mV_{p-p}, 1 kHz signal.
   d. Return the oscilloscope volts/division setting to 10 V/division.
   e. Disconnect the output of the PG 502 from the oscilloscope and connect it to the EXT TRIGGER IN connector on the MPU board.
   f. Connect channel 1 of the oscilloscope to the EXT TRIGGER OUT connector on the MPU board.
   g. Short the outside ring of the EXT TRIGGER IN connector to the outside of the BNC connector (see Figure 5-2).
   h. Check for a 4 V_{p-p}, 1 kHz signal at the EXT TRIGGER OUT connector.
   8. Disconnect the coaxial cables.

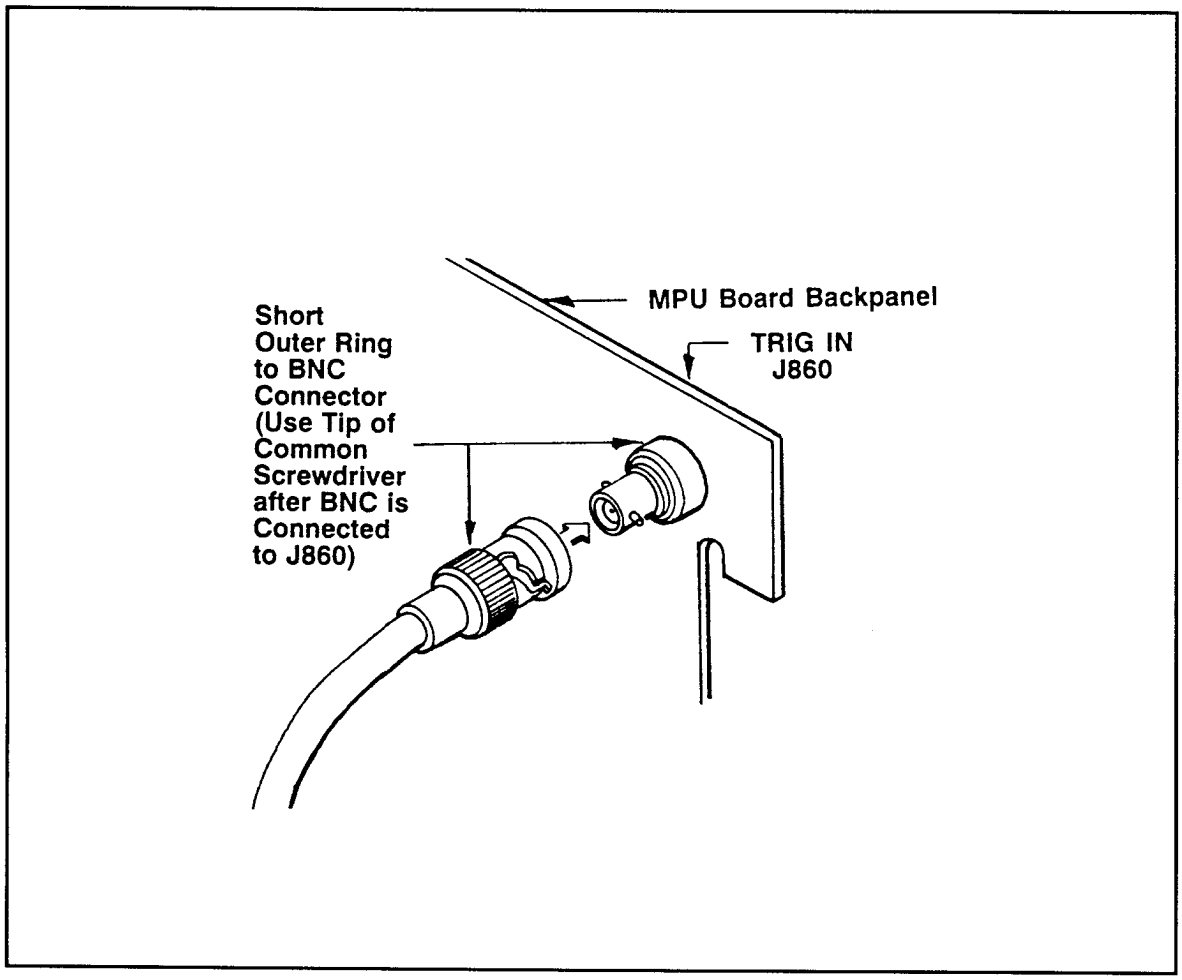


Figure 5-2. Testing the 10X TRIG IN circuit.

ADJUSTMENT PROCEDURES

Introduction

The 2 Mbyte RAM version of the MPU board (Tektronix part numbers 671-0058-00 through 671-0058-10 or 671-0058-50 through 671-0058-54) includes three adjustments:

1. Clock Calendar Oscillator Adjust
2. Three-volt ECL Termination Voltage Adjustment
3. SYSTRIG Signal Comparison Adjust

The 4 Mbyte RAM version of the MPU board has only two adjustments:

1. Three-volt ECL Termination Voltage Adjustment
2. SYSTRIG Signal Comparison Adjust

In addition, a procedure for setting the "day," "month," and "time" is provided.

The following adjustment procedures are written assuming that the MPU board is connected to other mainframe components, that the board is in the servicing position to allow access to the adjustments, and that the instrumentation system is powered-on. Refer to Section 6 in the applicable mainframe service manual for instructions on how to position the MPU board for servicing.

Loading Diagnostics Software

Diagnostic software is used when adjusting or checking the Clock Calendar Oscillator and using the Time/Date routine to set the day, month, and time. Use the following procedure to load the diagnostics software into the RAM on the MPU board:

1. Insert the diagnostic floppy disk.

NOTE

If you already have diagnostics software in a DIAG directory on your hard disk, you can load diagnostics from the hard disk. If you suspect the diagnostics on the hard disk is corrupt, insert the floppy disk with the diagnostics software.

2. Access the Save/Restore menu by pressing Util, then scroll through the menus until SAVE/RESTORE is selected.
3. In the operation portion of the Save/Restore menu, select Load Application as the operation.
4. Select the following in the parameter portion of the Save/Restore menu:

Source Disk	FLOPPY or HARD
Source Directory	DIAG
Source File	DIAG_MAN
Destination Module	SYSTEM

5. Press F1: Execute Command to load the diagnostics software. A message on the top line of the display tells you when the load operation is complete.
6. Select the Diagnostics menu by scrolling through the Utility menu.
7. Select CPU in the Module field and the appropriate test in the Area field.
8. Move the cursor to the Routine field. The cursor must remain in this field to EXECUTE the selected operation.
9. Start the operation by pressing F2: Run Selected.

Clock Calendar Oscillator Adjust

This adjustment ensures that the calendar clock oscillator is set to meet performance requirements. Proceed as follows (Refer to Figure 5-1 to locate probe test points):

1. Set the 2467B Oscilloscope (with Option 06 or 09) to measure the period of the Calendar Oscillator. Set the controls of the oscilloscope as follows:

Input Sensitivity	1 V/division
Input Coupling	DC
Display Mode	CH 1
Timebase	20 ns/division
Trigger Mode	NORMAL
	INT (Internal)
	DC Coupling
Trigger Source	CH 1
Trigger Slope	– (Negative)

2. Connect the channel 1 probe to J460 on the MPU board. See Figure 5-1 for location of J460.
3. Select M Clock Adjust in the Area Field of the Diagnostics menu and move the cursor to the Routine field. See *Loading Diagnostics Software* earlier in this section if you need further instructions.
4. Press F2: Run Selected.
5. Check for a period measurement between 0.99993 and 1.00007 seconds if you have the MPU board with 4 Mbyte RAM, or between 0.9997 and 1.0003 seconds if you have a MPU board with 2 Mbyte RAM. On the 2 Mbyte RAM version of the MPU board, you can adjust C455 (see Figure 5-1 for location) for a period of 1.0000 ± 0.0003 second.
6. Press F1: STOP to exit the test.
7. Disconnect the probe from the MPU board.

Set Time/Date Procedure

Use the following procedure to set the "Day," "Month," and "Time" of the clock calendar:

1. Select M Set time/date in the Area field of the Diagnostics menu. See *Loading Diagnostics Software* earlier in this section if you need further instructions.
2. Move the cursor to the Routine field and press F2: Run Selected.
3. Follow the displayed instructions to set the date and time. Observe that the seconds portion of the displayed setting is changing to verify that the system is operating properly.
4. Press F8: Exit to exit the test.

Three-Volt ECL Termination Voltage Adjust

Plus three volts is used as an ECL termination voltage for selected TekLink circuits. Use the following procedures to adjust the ECL voltage (See Figure 5-1 for test point and adjustment locations):

1. Set the DM502A Digital Multimeter to 2 V range of the DCV function.
2. Connect the High (positive) lead of DMM to the left end (nearest to the edge of the circuit board) of C506.
3. Connect the Low (negative) lead of DMM to right end of C506.
4. Adjust R500 for a reading of 2.000 ± 0.025 V.
5. Disconnect the DMM leads from the MPU board.

SYSTRIG Signal Comparison Adjust

Use the following procedure to set the compare input of U753B to 0.0 VDC (see Figure 5-1 for test point and adjustment locations):

1. Set DMM to 200 mV on the DCV function.
2. Connect the Low (negative) lead of the DMM to the metal stiffener that is near the center of the MPU board.
3. Connect the High (positive) lead of the DMM to pin 10 of U753
4. Adjust R753 for a reading of 0.00 ± 2 mV.
5. Disconnect the DMM leads from the MPU board.

Section 6
DISASSEMBLY/ASSEMBLY

GENERAL INFORMATION

The MPU board consists of the electrical circuit board, electrical components, and miscellaneous mechanical parts.

Except for the removal/replacement of failed electrical components, there is no disassembly/assembly required for the MPU board. An exploded-view illustration in *Section 11: Mechanical Parts List* shows the physical assembly of the MPU board and miscellaneous mechanical components.

Instructions on how to remove/install an MPU board from/into a mainframe are contained in the applicable mainframe service manual.

Refer to *Section 7: Maintenance* for instructions on how to remove or replace the battery used by the calendar IC.

Section 7
MAINTENANCE

INTRODUCTION

This section contains the following information:

- Maintenance tools
- General maintenance precautions
- Preventive maintenance information
- Corrective maintenance information

MAINTENANCE TOOLS

The tools most often needed when servicing an MPU board are those typically found in an electronic technician's tool kit. Special tools and supplies include:

- 15 W soldering iron
- 60/40 rosin core solder
- IC desoldering tool

MAINTENANCE PRECAUTIONS

WARNING

Be sure to observe standard electrical precautions if the MPU board is in the service position when connected to other instrument modules (application modules, power supply, disk drives, etc.). Dangerous electric-shock and mechanical hazards may be exposed when mainframe and power supply covers are removed. The fan is also exposed. Section 6 in the applicable mainframe service manual describes how to place the MPU and acquisition modules in service positions.

Soldering

Most electrical components are soldered in place.

CAUTION

If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

Refer replacement of soldered multi-pin gate arrays to a Tektronix service center where appropriate desoldering tools are available.

The flux in solder may leave a residue on the circuit board that can provide a high-resistance leakage path and affect electrical operation. Be sure to clean off this residue with isopropyl alcohol.

Static Precautions

CAUTION

Static discharge can damage any semiconductor on this circuit board.

Observe the following precautions to avoid damage:

- Minimize handling of static-sensitive components.
- Transport and store static-sensitive components in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive components.
- Discharge static voltage from your body by wearing a wrist strap when handling these components. Servicing static-sensitive components should be performed only at a static-free workstation by qualified service personnel.
- Don't put anything capable of generating or holding a static charge on the workstation surface.
- Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
- Keep component leads shorted together whenever possible.
- Pick up components by the body, never by the leads.
- Do not slide components over any surface.
- Use a soldering iron that is connected to an earth ground.
- Use only special anti-static suction type or wick desoldering tools.

NOTE

Damage to electrical components may not be immediately apparent. Always follow the precautionary measures previously listed when handling static-sensitive components.

AC Voltage Select Switch

CAUTION

Be sure that the VOLTAGE SELECT switch on the mainframe's power supply and the Color CRT monitor are set for the AC voltage being used. If not set to match the AC voltage, power supplies can be damaged.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of periodic cleaning and inspection. Accumulation of dust on components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown. Periodic cleaning and inspection reduces instrument breakdown and increases instrument reliability.

Cleaning

The MPU board and associated modules should be cleaned as often as the operating environment requires. A convenient time to perform these procedures is immediately prior to troubleshooting or other maintenance-related activity. Perform these procedures more often if required by the operating environment.

CAUTION

Cleaning should be done with a dry, low-velocity stream of air and a soft-bristle brush. If liquid cleaning is necessary, spray-wash dirty parts with isopropyl alcohol, denatured ethyl alcohol, or a solution of 1% mild detergent and 99% de-ionized water. Then, use de-ionized water to THOROUGHLY WASH all parts. IMMEDIATELY DRY all parts with a low speed air blower.

DO NOT use fluorocarbon-based spray cleaners or chlorinated hydrocarbon cleaners; they may damage the circuit board material or plastic parts, and they may leave a dust-collecting residue.

To prevent damage from electrical arcing, ensure that all circuit board connectors are completely dry. Do this by heating the board in an oven at 60°C (160° F) for 30 minutes before installing into a mainframe and applying power.

Inspection

Inspect internal modules for broken connections, poorly-seated components, leaking capacitors, damaged hardware, and heat-damaged components.

Repair any obvious problems. However, take particular care if you find any heat-damaged parts. Overheating usually indicates other circuit problems. To prevent recurrence of the damage, find and correct the cause of the overheating. Note that replacement of electrical components may necessitate readjustment of circuitry. Refer to the *Replaceable Electrical Parts,* Section 9 for a list of part and component descriptions.

CORRECTIVE MAINTENANCE

Corrective maintenance includes the following:

- Obtaining replacement parts
- Circuit board pin replacement

Obtaining Replacement Parts

Electrical and mechanical parts for the MPU board can be obtained through your Tektronix field office or representative. However, many of the standard electrical components can be obtained locally. Before purchasing an ordinary part, check the *Replaceable Electrical Parts* section for a listing of value, rating, and description.

NOTE

Check the parts lists before replacing electrical components. If the part is called out as screen or burned-in, the replacement part must also be screen or burned-in or the repair will not be effective.

When selecting replacement parts, remember that the size and shape of a component may affect its performance. All replaceable parts should be direct replacements.

Some of the mechanical and electrical parts are manufactured by Tektronix. Other parts are manufactured for Tektronix to satisfy particular design requirements or certain specifications. To determine the manufacturer of a part, get the MFR CODE (manufacturer's code number) from the electrical or mechanical parts list and refer to the Mfr Code Number to Manufacturer Cross Index at the beginning of the Replaceable Electrical or Mechanical Parts List.

When ordering replacement parts from Tektronix, include the following information:

- Instrument type
- Instrument serial number
- Description of the part (if electrical, include the component number)
- Tektronix part number

Circuit Board Pin Replacement

On occasion, it may be necessary to repair a circuit board connector pin. A circuit-board pin replacement kit, including the necessary tools, instructions, and replacement pins with attached spare ferrules, is available from Tektronix. Contact your Tektronix Service Representative for ordering information.

CAUTION

Use extreme care when replacing circuit-board pins. Most circuit boards have conductive paths between the top and bottom board layers. All soldering, removal, and re-insertion of pins must be done with care to prevent breaking any electrical paths on the board.

Refer to Figure 7-1 when performing the following pin replacement procedures:

1. Use a 15 W soldering iron to unsolder the pin while pushing it out of the board with a pair of pliers. If the pin is too short to use pliers, push it out with any round device not over 0.28 inches in diameter.
2. If the ferrule remained in the board, go to Step 3. If the ferrule came out with the pin, go to Step 4.
3. If the ferrule remained in the board, do the following:
   a. Carefully ream out the solder with a 0.31 inch drill.
   b. Remove the ferrule from a new pin and insert the new pin into the old ferrule in the same position as the old pin.
   c. Go to Step 5.
4. If the ferrule came out with the pin, do the following:
   a. Clean the excess solder out of the hole with a solder-removing wick and a scribe.
   b. Insert the new pin with ferrule in the same position as the old pin.
   c. Go to Step 5.
5. When the new pin is properly placed, carefully solder it on both sides of the board.
6. Clean any remaining residue from the board according to the cleaning instructions given earlier in this section.

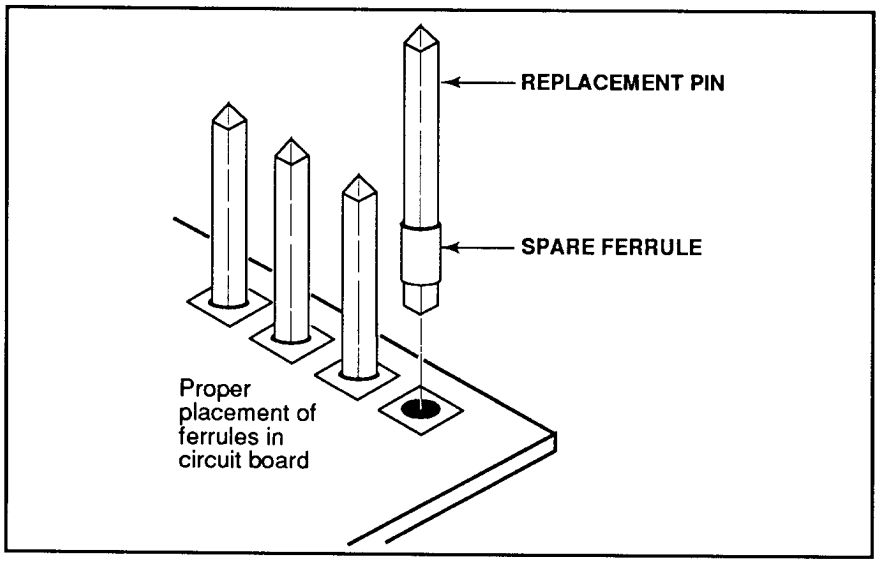


Figure 7-1. Circuit board pin replacement.

CALENDAR IC BATTERY REPLACEMENT

A lithium battery is used to power the clock-calendar IC. Lithium batteries have a useful life of about three years and therefore must be replaced on a periodic basis. Battery voltage should be checked on both a periodic basis and whenever the calendar appears to be functioning in an abnormal manner. Use the following procedures to (1) determine the condition of the battery, and (2) remove/install a battery.

Testing the Battery

The calendar battery is a 3.0 volt, lithium battery placed in a socket on the MPU board. If the battery voltage drops below 2.6 volts, data stored in the Calendar IC may be lost. Also, if the battery voltage is too high, it may cause indeterminate effects. To check the battery voltage, use the following procedure:

1. Remove power from the MPU board.
2. Connect the positive lead of a voltmeter to the + (positive) side (exposed side) of the calendar battery BT275 and negative lead to pin 14 of U350 (see Figure 7-2).
3. Check for a voltage reading between 2.6 V and 3.2 V. If the reading is outside these limits, replace the battery. See the following *Battery Replacement Procedure*.

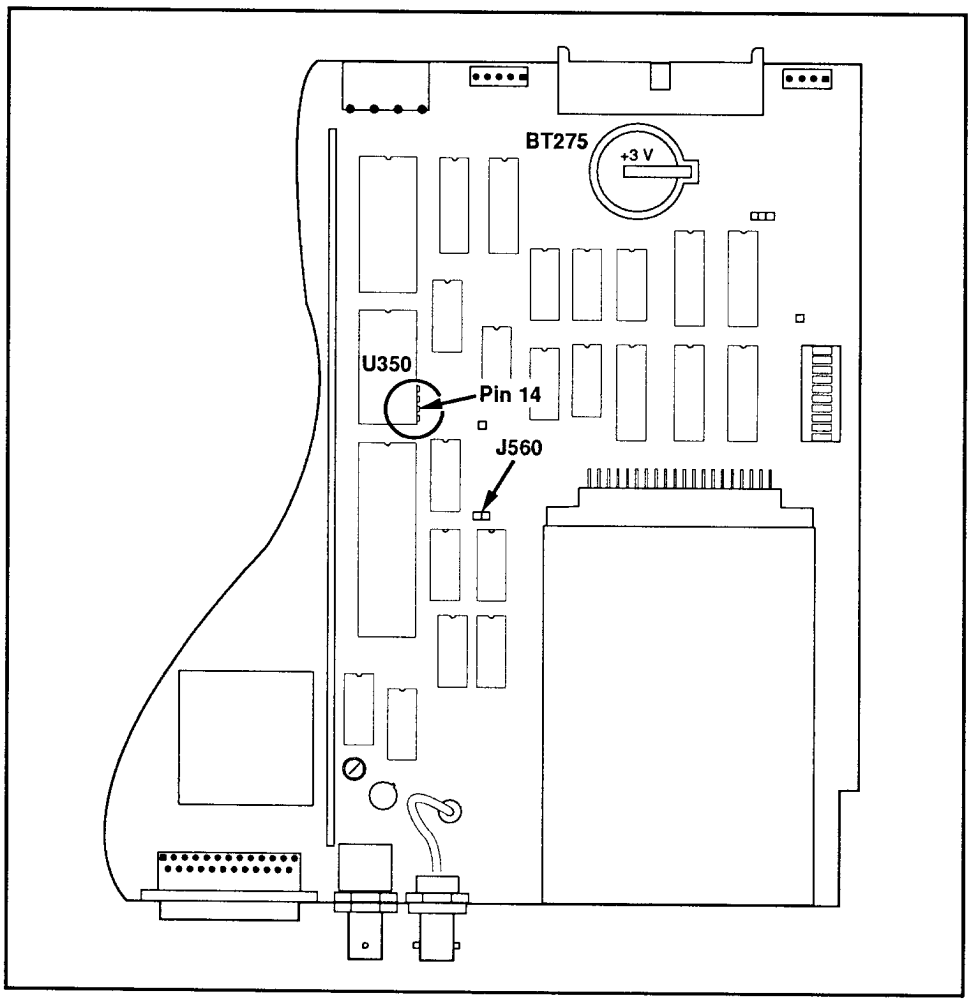


Figure 7-2. Battery check test points.

Battery Replacement Procedure

Whenever it becomes necessary to replace the battery, use the appropriate part. Refer to *Section 10: Electrical Parts List* for battery part number.

WARNING

To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. DO NOT recharge, crush, or disassemble the battery. DO NOT incinerate or heat the battery above 212° F (100° C). DO NOT expose contents of battery to water.

To avoid personal injury, observe the proper procedures for handling and disposal of lithium batteries given below.

Dispose of batteries in accordance with local, state, and national regulations. Typically, small quantities of batteries (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill. Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting and they must be packed in a sturdy container that is clearly labeled "Lithium Batteries—DO NOT OPEN."

Use the following procedure to replace the battery.

1. Using a small common screwdriver, or similar blunt tool, gently pry up the arm clamp that holds the battery in its socket. Tilt the board slightly and the battery will slide from the socket.
2. Install the replacement battery by inserting it under the arm clamp and gently pushing the battery into the socket. Be sure to observe polarity (positive side of the battery contacting the arm clamp).
3. Check battery voltage as described under *Testing the Battery*.
4. Apply power to the MPU board and program the calendar. Refer to *Set Time/Date Procedure* in *Section 5: Verification and Adjustment Procedures*.

Section 8
TROUBLESHOOTING

SCOPE OF TROUBLESHOOTING INFORMATION

Information in this section helps a technician locate a hardware failure on the MPU board. Information is not limited to the MPU board. As needed, references are made to other system modules, and/or manuals to help you determine if circuitry on the MPU board or other modules may be at fault. The order of presentation is intended to follow the information needed to "bring up" a "dead" instrument. Information is organized under the following subjects:

- *General Information* lists the type of equipment needed for troubleshooting, troubleshooting precautions, and placement of modules for troubleshooting.
- *Troubleshooting Guidelines and Information Locater* guides you to troubleshooting and diagnostic information related to the problem area. Here you are directed to specific troubleshooting information for each replaceable system module.
- *System Power Troubleshooting* describes what to check when a system will not power-up, and what to check when a system develops a "thermal" condition.
- *Power-On Boot Sequence (Self-Verification)* describes the system verification process that occurs each time the system is powered on. Here you are again directed to additional troubleshooting information related to the nature of a power-on failure.

GENERAL TROUBLESHOOTING INFORMATION

Troubleshooting Equipment

The following equipment, or equivalent, is recommended for troubleshooting the MPU board and associated modules.

- Tektonix 1240 Logic Analyzer
- Tektronix 2467B Oscilloscope with two P6136 probes
- Tektronix DM 502A Digital Multimeter
- Tektronix TM 502A Power Module
- ASCII terminal
- System diagnostic software

Tools required to service the analyzer are those commonly found in an electronic technician's tool kit.

Troubleshooting Precautions

Component Handling

If the MPU board is repaired to a level lower than board or module replacement, refer to Section 7 of this manual for cautionary guidelines and recommended practices regarding special handling required for static sensitive devices.

CAUTION

Static discharge can damage any semiconductor component in this Module.

The Color Display Monitor

Refer servicing of the color monitor to qualified service personnel. Be sure to observe the following precautions when working on the CRT:

CAUTION

CRTs RETAIN HAZARDOUS VOLTAGES FOR LONG PERIODS OF TIME AFTER POWER-OFF. The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

BEFORE ATTEMPTING ANY WORK ON THE CRT, discharge the CRT by shorting the anode connection to chassis ground using a plastic-handled screwdriver. When discharging the anode, place the screwdriver against chassis ground, then slip the screwdriver tip under the CRT anode cup.

USE EXTREME CAUTION WHEN HANDLING THE CRT. Rough handling may cause it to violently implode. Do not nick or scratch the glass or subject it to undue pressures during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

PHYSICAL PLACEMENT OF MODULES FOR TROUBLESHOOTING

Refer to Section 6 of the applicable mainframe service manual for illustrations that show the relative positions of the electronic circuit modules in the mainframe. Section 6 (in the mainframe service manuals) also describes how to position the mainframe circuit boards for troubleshooting.

TROUBLESHOOTING GUIDE AND INFORMATION LOCATOR

Introduction

The following describes how to approach a troubleshooting task. This approach assumes that a system malfunction or fault condition is evident. From this, you are directed to detailed troubleshooting information that will usually isolate the problem to the failed module, circuit, or circuit component.

Troubleshooting Guide

Different failures often require different troubleshooting approaches. For example, if failures are detected during the power-on sequence, you may choose either to perform additional diagnostic tests or to bypass further diagnostics (if failures are acceptable, e.g., failures in acquisition modules that are not being used). If the mainframe cannot produce a screen display you must use other methods to troubleshoot the malfunction. The following text outlines general fault conditions and the appropriate troubleshooting approach/method for each.

1. First, analyze the failure symptoms. Keep in mind that at one time, the unit was operational -- even a unit that is dead on arrival (DOA).

   For DOA instruments, check the obvious (power cord, mains supply, mains fuse, and internal cabling. (Cables may loosen in transit.)

2. Does the unit power-on (is the STANDBY/ON LED lit)?

   If not, refer to *System Power Troubleshooting*.

3. The unit powers on but there is no start-up menu (or no displayed data at all). In this case, check the Diagnostic LEDs on the MPU board. If an error is indicated, there is a problem with the MPU kernel circuitry. Refer to *Kernel Diagnostics Tests* later in this section for detailed information.

4. If there is no display and no failure indicated by the Diagnostic LEDs, then suspect a failure either in the video control circuitry or in the display module itself. For external-mounted display modules, check the interconnect cable to ensure it is properly connected. If OK, then refer to the appropriate mainframe service manual for more detailed troubleshooting information regarding your display module.

5. The STANDBY/ON LED lights, and there is a start-up menu displayed. This indicates that the MPU kernel and associated circuits are OK, as the boot process was able to pass power-on diagnostic tests and boot the operating system from the system disk.

6. If the unit was in a powered-on condition, at what point did the failure occur?

   If the failure occurred DURING NORMAL OPERATION (expect either an over-voltage condition or circuitry failure), check the following:

   a. Check cooling vents for blockage, remove any blockage; then, after equipment has cooled down, recycle power. If unit powers on and displays the startup display, then problem was probably cooling. If problem occurs again during normal operation (after ensuring that cooling vents are cleared), then remove top cover and troubleshoot over-temperature condition. Refer to *System Power Troubleshooting* later in this section.

   b. After recycling power and the power supply appears to come up (as indicated by STANDBY/ON switch being lit), but there is no display, then check the Diagnostic LEDs on the MPU board. If an error is indicated, there is a problem with the MPU kernel circuitry. Refer to *MPU Kernel Diagnostics Tests* for detailed information.

7. Unit powers on, displays startup menu but when you use the system it appears not to be operating correctly.

   a. Check operational procedures according to Users manual(s).

   b. Load System Diagnostics Software and exercise all tests or selected tests. (Refer to Section 9 for operational guidelines and test descriptions.) After you run diagnostic software, you should have a good idea which area of circuitry on the module has failed.

For additional troubleshooting information refer to *Information Locater* immediately following and to *Theory of Operation*, Section 4 (this manual).

Information Locater

Not all troubleshooting and diagnostic information is located in this section. For example, each mainframe service manual contains additional troubleshooting information for each system module. The following describes the location of troubleshooting information for each replaceable system module.

Keyboard or Control Panel Module

The MPU board may be connected to an ASCII-type keyboard or a control panel module depending on the type of mainframe in which the MPU Board is installed. If the Keyboard or control panel is suspected to be faulty (intermittent keys, etc.), then refer to MPU Module Tests in Section 9 and run the *Manual Keyboard* test. This test produces a graphic display of the keyboard or control panel. When you press a key the corresponding screen key reverses video. Each key, and the scrolling knob, can be checked in this manner.

If the Keyboard or control panel do not work at all, then suspect either the interconnect cable, power, or the hardware circuitry. Refer to Sections 4 and 8 in the applicable mainframe service manual for keyboard or control panel theory and troubleshooting information, respectively.

Keyboard or Control Panel Interconnect Cable. Refer to the Keyboard or Control Panel Interconnect Diagram in Section 10 of the applicable mainframe service manual. Check the cable for opens and shorts. If bad, replace the cable. Refer to Section 6 in the applicable mainframe service manual for cable replacement procedures.

Keyboard or Control Panel Power. The keyboard or control panel receives +5 VDC power from the MPU board. Check the +5 V fuse on the MPU board and replace if needed. See Figure 8-1 for fuse location.

Keyboard or Control Panel Circuitry. If keyboard or control panel circuitry has failed, replace the module.

Disk Drive Module

The System Diagnostics software provides low-level tests for both the floppy and hard disk controller circuits as well as read and write tests for the disk drives. Refer to *MPU Module Test Descriptions* in Section 9 for test descriptions.

Both the floppy and hard disk drives receive power from the MPU board. Refer to the disk interconnect schematics in Section 10 of the applicable mainframe service manual for power cable routing. Refer to Figure 8-1 for fuse locations.

If a drive unit failure is suspected, refer to the drive descriptions in Section 4 of the applicable mainframe service manual. With the information provided there and with the interconnect diagram you should be able to confirm whether the disk drive or interconnect cabling is at fault. If the drive is bad, return the drive to Tektronix for repair and/or replacement.

Color Display Monitor Module

The diagnostics software provides a display test that verifies the operation of the MPU board's display controller circuitry. Refer to *MPU Module Test Descriptions* in Section 9 for detailed procedures.

Refer to Sections 4 and 8 of the applicable mainframe service manual for additional information regarding the color CRT monitor.

Flat Panel Display Module

The diagnostics software provides flat panel test patterns to verify the operation of the MPU board's display controller circuitry. Refer to *MPU Module Test Descriptions* in Section 9 for detailed procedures.

CAUTION

Do not connect the display cable with the Mainframe STANDBY/ON switch in the ON position. Doing so may blow F703 on the MPU board.

Fuse F703 may blow if you connect the display cable when the Mainframe STANDBY/ON switch is in the ON position. If the display is not operating when the STANDBY/ON switch is in the ON position, check for +12 VDC at J820 pin 1. If no +12 VDC at pin 1, turn off power and remove the power cord from the Mainframe. Disassemble the Mainframe to remove the MPU board and check the condition of F703. (Refer to Figure 8-1 for location of fuse on MPU board.)

The Flat Panel Display module consists of two electrical subassemblies, a Power Converter circuit board and the display device with attached circuit board. If the display device and/or its attached circuit board have failed, then return the complete Flat Panel Display module (including Power Converter board) to Tektronix for replacement and/or repair. If the Power Converter board is known to have failed, it can be replaced. Refer to Section 6 in the applicable mainframe service manual for instructions on how to remove the Power Converter board. Refer also to the description of the Flat Panel Display module in Section 4 of the applicable mainframe service manual. For signal interconnect information, refer to the Display Interconnect Diagram in Section 10 of the same manual.

Flat Panel Display Module Power The Flat Panel Display module receives power from the MPU board. DC power for the Flat Panel module is fused on the MPU board. Refer to Figure 8-1 for fuse location.

COMM Packs

The Diagnostics Software provides tests for the various 1200-Series COMM Packs. Refer to *COMM Pack Module Tests* for detailed information. In addition, each 1200-Series COMM Pack has its own manual. Refer to the relevant COMM Pack service manual for detailed service information.

The *Section 4: Theory of Operation* provides a detailed description of the COMM Pack Interface circuitry on the MPU board.

COMM Pack Power. COMM Packs receive +12 VDC and -12 VDC power distributed by the MPU board. Refer to the Interconnect Diagram in Section 10 of the applicable mainframe service manual for power interconnects . Refer to Figure 8-1 for fuse locations.

DUART RS-232C Ports

There are two possible RS-232C ports available. One is provided via an RS-232C COMM Pack plugged into the COMM Pack connector. The other port is via the DUART. (The Keyboard uses one side of the DUART, and the RS-232C port uses the other side.)

Diagnostics Software contains verification and fault isolation tests for the RS-232C circuitry. Refer to *MPU Module Test Descriptions* and to the Keyboard description in *Section 4: Theory of Operation* for detailed information (the description of the DUART's RS-232C host port is part of the functional description for the keyboard port).

Acquisition Modules

Software Diagnostics provide verification and fault isolation tests for troubleshooting the acquisition modules. Acquisition modules are also supported with their own service manuals. Refer to the descriptions of the diagnostic software in the applicable acquisition module service manual for test descriptions and for other troubleshooting and service information.

Power Supply Modules

Power supplies are different for each mainframe. Power supplies provide power directly to the MPU board and acquisition modules installed in a mainframe. Power for MPU peripheral modules is routed from and fused-protected on the MPU board.

There is no system diagnostic test to check the operation of a power supply. Refer to *System Power Troubleshooting* immediately following in this section for additional troubleshooting information. Also, refer the appropriate mainframe service manual for service strategy and other service information relevant to a particular power supply.

SYSTEM POWER TROUBLESHOOTING

There are several things to keep in mind when troubleshooting a system power problem.

First check the obvious:

- AC line cord properly installed
- Front panel STANDBY/ON switch in ON position (lighted)
- Rear panel line selector switched to proper position
- Rear panel AC line fuse in good condition

If the obvious checks do not identify the problem, then the following information may prove helpful.

Power Distribution

The Power Supply module distributes +5 VDC, +12 VDC, and -12 VDC supplies to the MPU board and up to two acquisition modules. All modules (except acquisition modules) that connect to the MPU board receive their power via the MPU board. Refer to the Power Interconnect Diagram in the Section 10 of the applicable mainframe service manual for power distribution.

Fuses

The MPU board provides fuse protection between the MPU circuits and connected modules. The electrical schematics for the MPU board show these fuses. Table 8-1 shows on which schematic sheet the fuses are located, and Figure 8-1 shows where the fuses are located on the MPU board.

Table 8-1
Fuse/Schematic Sheet Location

Fuse	Value	Schematic Sheet	Voltage	Used By
F110	1.5 A	11	+5 V	Keyboard/Console
F240	3.0 A	20	+5 V	HD Drive & Aux Fan
F250	1.5 A	20	+5 V	HDC Board
F255	3.0 A	20	+12 V	HDC Board
F286	1.5 A	10	+5 V	Floppy Drive
F470	1.5 A	4	+5 V	COMM Pack
F471	1.5 A	4	–12 V	COMM Pack
F575	1.5 A	4	+12 V	COMM Pack
F700	0.75 A	15	–12 V	Expansion Board
F701	0.75 A	15	+12 V	Expansion Board
F702	0.75 A	15	+5 V	Expansion Board
F703	5.0 A	14*	+12 V	Display Unit
F825	5.0 A	14†	+12 V	Display Unit

**MPU Board, 671-0058-01 and greater versions.*
†MPU Board, 671-0058-00 version only.

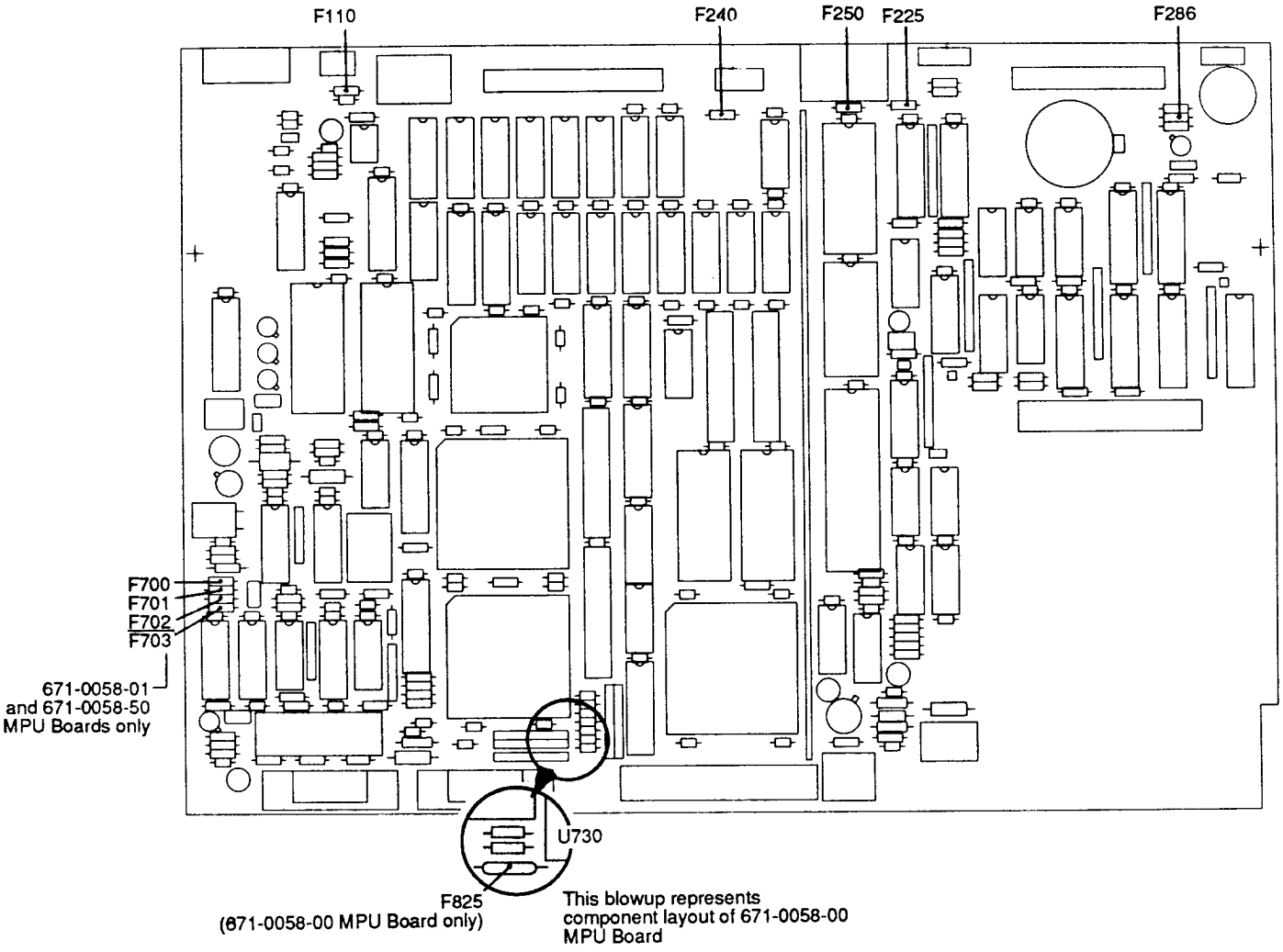


Figure 8-1. MPU board fuse locations.

Power Supply Troubleshooting Chart

Refer to the applicable mainframe service manual for detailed information about the mainframe power supply. All power supplies are field replaceable units and must be returned to Tektronix for repair.

When the previously-described troubleshooting items have been checked and the power supply refuses to come up, use the power supply troubleshooting chart in Figure 8-2. This chart will assist you in locating the problem area. Refer also to information, immediately following, titled *Troubleshooting Thermal Conditions.*

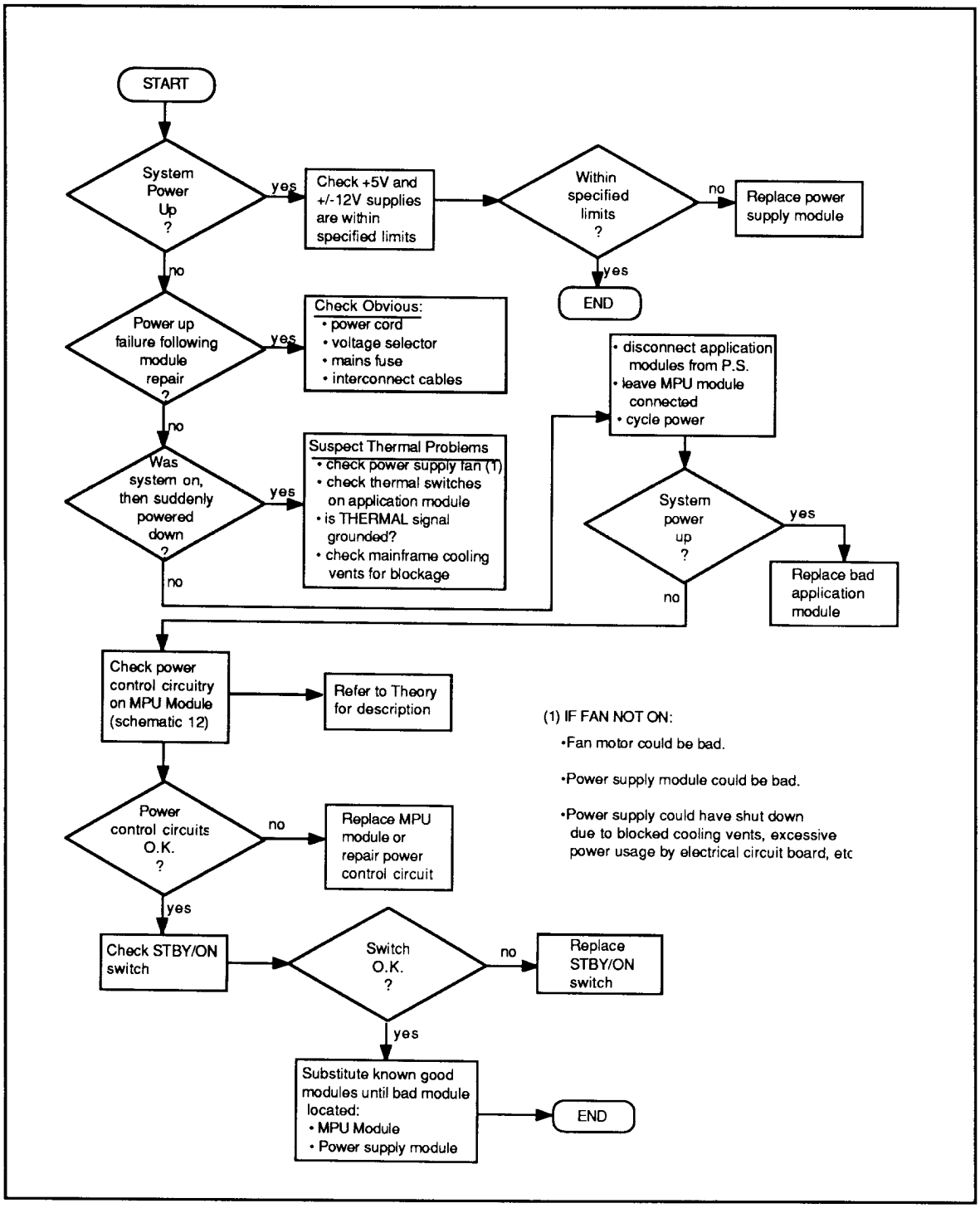


Figure 8-2. Power supply troubleshooting chart.

Figure 8-3 shows power supply test points on the MPU board.

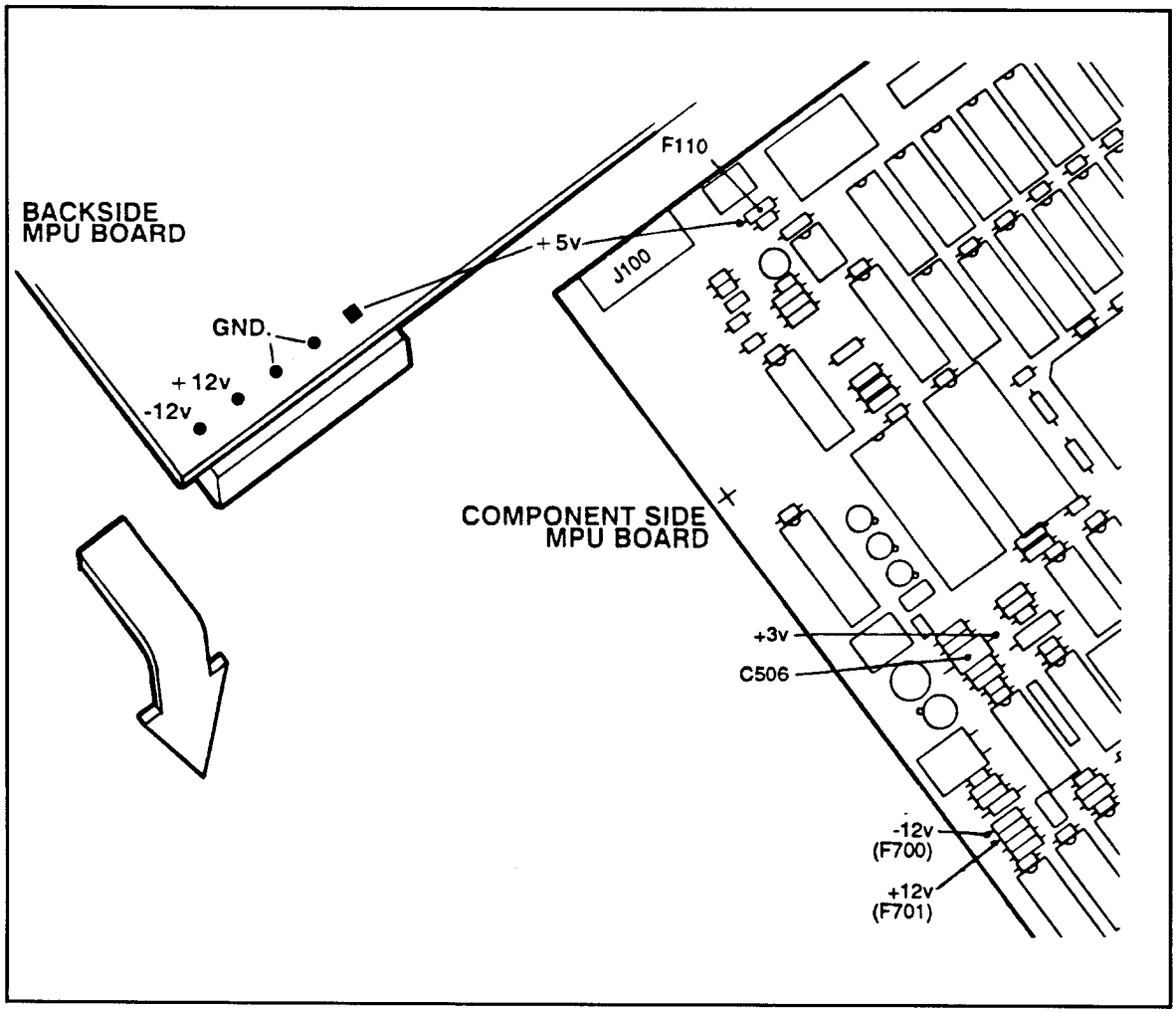


Figure 8-3. Power supply test points.

Troubleshooting Thermal Conditions

If air flow is insufficient, ambient temperature rises inside the mainframe enclosure. An over-temperature condition can be caused by any of the following:

- Cooling vent obstruction
- Fan failure
- Fan voltage too low
- Excessive drain on power supply

Most acquisition modules use thermal switches to protect critical circuits on the module. If the ambient temperature exceeds the thermal rating of a switch, the switch will short to ground. This action grounds the THERM signal, shutting down the power supply via the power control circuit on the MPU board. Any acquisition module connected to an MPU board can shut down the mainframe power supply in this manner. Figure 8-4 shows how a thermal switch is wire-ORed to the MPU's THERM signal line.

Refer to the applicable acquisition module service manual for location of thermal switches. Once a suspected switch is located, cool it with cool spray and recycle power. If the system powers-on, then strongly suspect an excessive temperature problem. Check the problem further by ensuring that all cooling vents are cleared of obstructions before operating the instrument. If the power supply fails again, suspect faulty circuitry. The thermal switch may be bad or circuitry in the area of the thermal switch may be using excessive power. Low-level troubleshooting is needed.

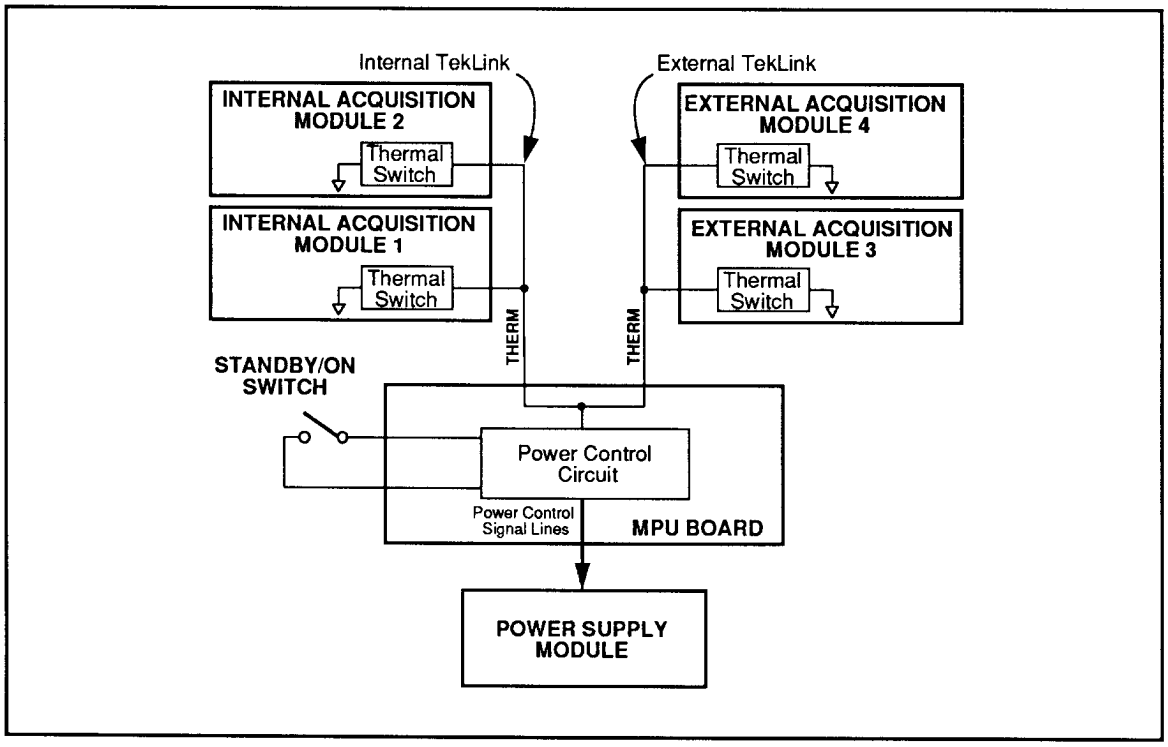


Figure 8-4. Thermal sensor wiring.

POWER-ON SEQUENCE (SELF-VERIFICATION)

Overview

The MPU board is supported with power-on boot code that:

- Verifies MPU kernel circuitry
- Boots the operating system
- Loads the application software

A power-on failure causes related diagnostic LED and/or display error messages that, upon interpretation, will either state the failure or guide you to more detailed troubleshooting/diagnostic information.

The following is a description of the power-on sequence. Use this information to help troubleshoot a power-on sequence failure.

Troubleshooting The Power-On Sequence

The following is a description of what the system does during the power-on sequence. If the system is not performing as described, suggestions are given as to what the problem may be. Figure 8-5 shows the power-on sequence and recommended action for a technician should a power-on failure occur.

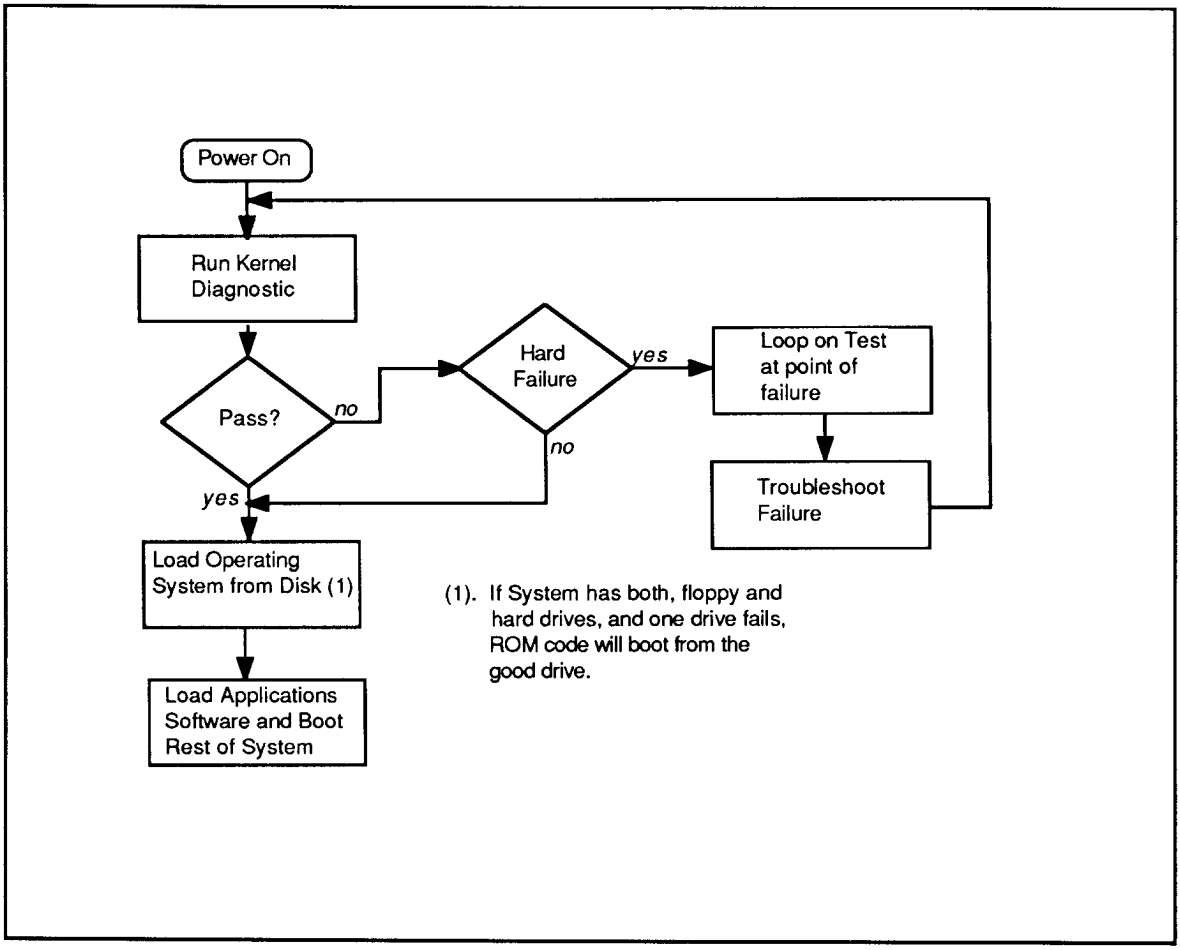


Figure 8-5. Power-on sequence.

The major steps of the power-on sequence are (refer to Figure 8-5 as needed):

1. Immediately following the application of power (or a reset function) the information in Figure 8-6 appears on the display monitor. It states that kernel diagnostics have started, and it lists the tests and the pass/fail indication for each.

   If the kernel diagnostic display indicates that a kernel test failed, identify the test either by name or by LED code. Refer to Table 8-2. (Also refer to information under the heading *Interpreting the LED Code*, then refer to *Troubleshooting Using Kernel Diagnostic Tests* later in this section for detailed troubleshooting information for the failed test.)

   If a failure is detected in the basic kernel circuits, the boot process halts and loops on the failed kernel test. It will not continue until the failure is repaired.

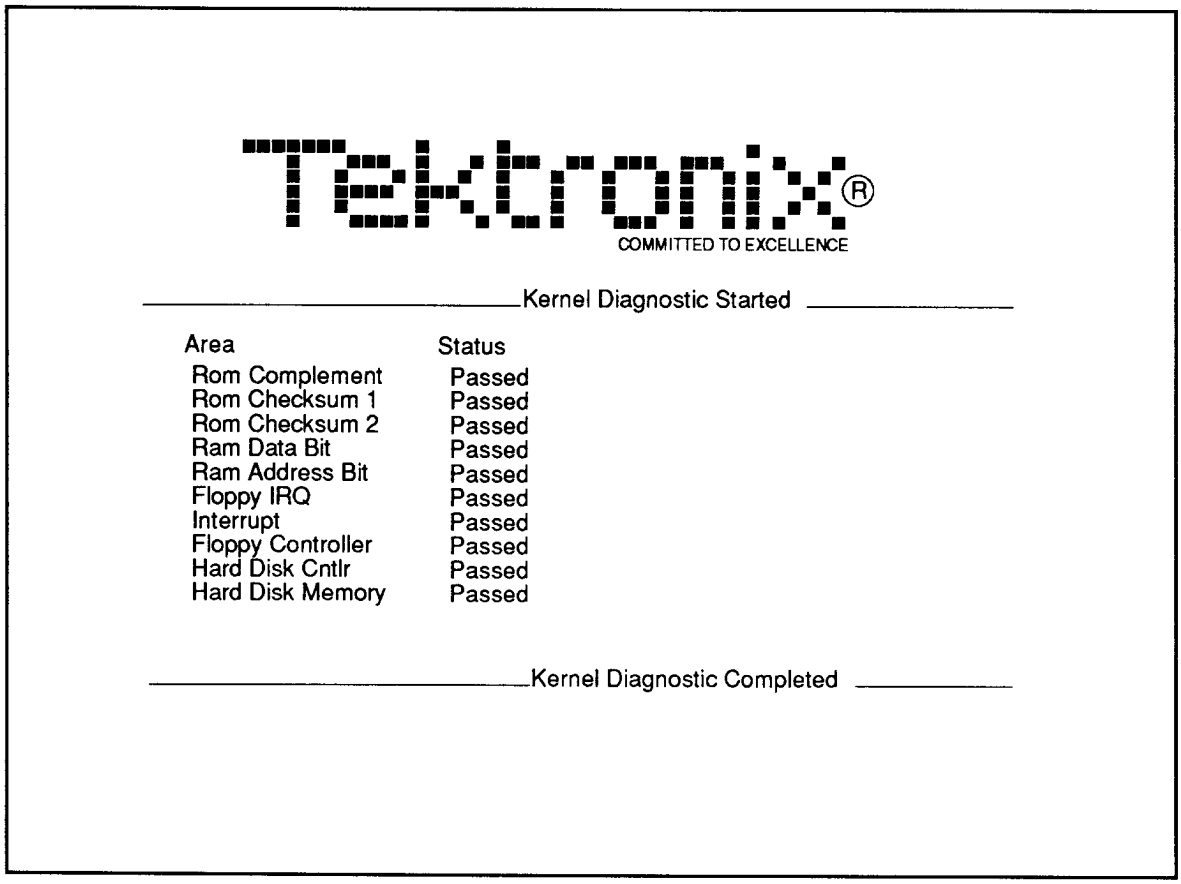


Figure 8-6. Displayed data indicating kernel diagnostics are in progress.

2. When all kernel tests have passed, the phrase "Kernel Diagnostics Completed" is displayed followed by "Booting From the Floppy (or Hard) Disk" and "Executing Code Loaded from Disk."

   An error during this phase of the boot process could cause one of the Diagnostic LED codes shown in Table 8-3. For 3000-Series products, it could also cause a diagnostic configuration error index code. This code will be displayed on the error line of the diagnostic menu display.

3. Boot code loads the acquisition software and the status menu is displayed.

KERNEL DIAGNOSTIC TESTS

Overview

As stated earlier, ROM-based test code runs automatically during the power-on sequence to test the functional integrity of the 68010 and associated "kernel" circuitry. The system will not boot if a kernel error is detected that will hinder the booting process.

The following provides a brief description of the following microprocessor compute kernel tests:

- ROM circuitry
- RAM circuitry
- Floppy interrupt circuitry
- Disk drive circuitry

ROM Verification Test

ROM is verified using a stackless ROM test. ROM is tested by first checking two locations with complimentary bytes (one byte contains 00, the other FF). This test ensures that the 68010 data bus can be driven high and low. Since the Data Bus is 16 bits wide, the two 256K ROMs will be tested together. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the failed location.

ROM Checksum Test

ROM Checksum Tests are performed on both the even ROM IC and the odd ROM IC. Odd and even checksum tests are performed on each IC. The calculated checksum is then compared to the checksum stored in the ROM "trailer."

RAM Verification Test

RAM is verified using a stackless RAM test. A walking bit test is used for data bit independence testing. (An alternating AA,55 pattern is used.) This provides complete testing and also provides a fast power-on process. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the failed location.

Floppy Interrupt Circuit Test

This test checks the floppy interrupt (FLOPPY_IRQ) signal. The GLUE gate array disables all interrupts at their source and then forces an active FLOPPY_IRQ from the floppy controller IC. Bit 10 of the GLUE interrupt status register (internal to the GLUE gate array) is then checked to determine if it is set (FLOPPY_IRQ asserted). The GLUE gate array then forces FLOPPY_IRQ off and checks that no other interrupt bits were set in the GLUE interrupt status register.

Disk Drive Verification Test

This test checks both floppy and hard disk controller circuitry and hard disk RAM. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the disk drive.

NOTE

This happens only if there is one drive installed, or if both the hard and floppy drives have problems.

Displaying Kernel Diagnostic Errors

Kernel diagnostics try to display an error in two ways: (1) by writing to a display monitor and by (2) displaying a failure code on a set of diagnostics LEDs. Any displayed error message is self-explanatory in regards to the name of the test that failed. Under some circumstances, messages will not be displayed on the display unit (e.g., if the display circuitry fails or if the nature of the failure is such that activating the display could crash the system). Error codes for kernel test failures are also displayed by the diagnostic LEDs.

The MPU board's diagnostic LEDs consist of 10 individual LED segments; eight segments indicate the progress of the kernel tests (power-on tests) and two segments indicate the status of the boot process. The diagnostic LEDs are shown in Figure 8-7.

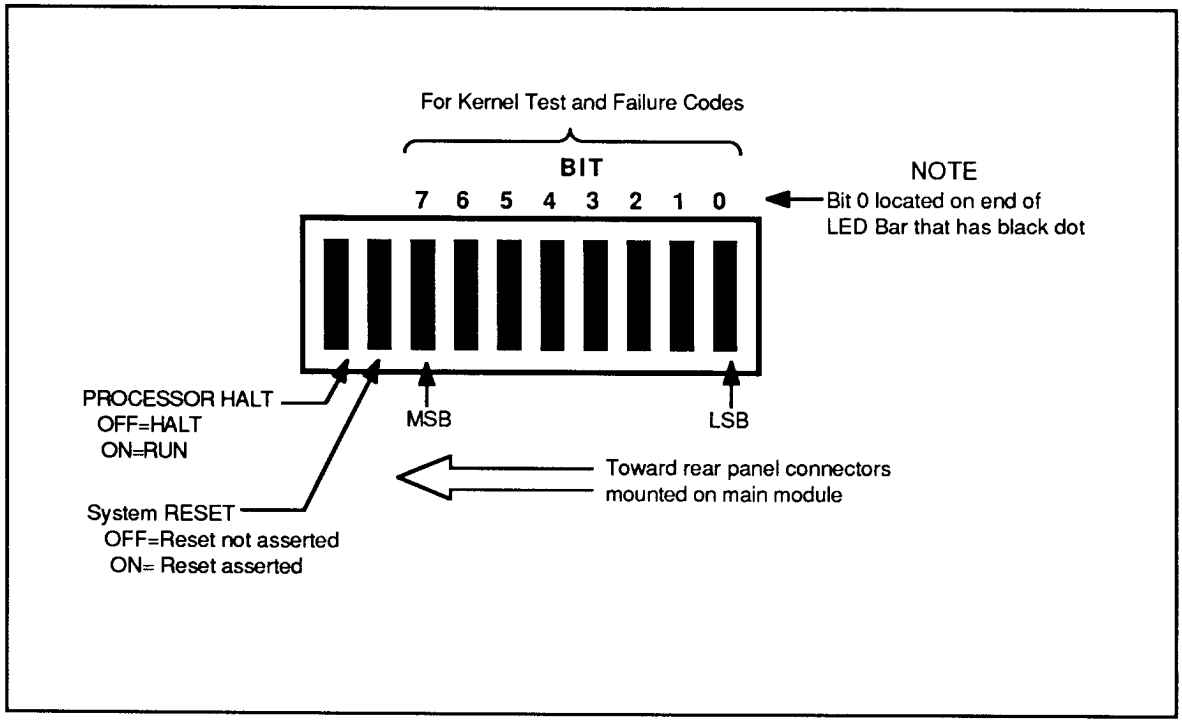


Figure 8-7. MPU board diagnostic LED (as viewed from component side).

The diagnostic LEDs are shown viewing the MPU board with component side up and with the board in the service position.

Interpreting the LED Codes

LED codes are represented in the following text by:

1 = LED segment is ON (lit)

0 = LED segment is OFF (not lit)

F = LED segment is FLASHING (alternating ON and OFF)

If the processor halts (HALT segment is OFF) due to a test failure, the LED segments will be either ON or OFF to indicate the fault error.

NOTE

Some segments will flash during certain tests, indicating an error has been detected. However, as long as the HALT segment is lit (processor not halted), the processor continues to execute instructions. Refer to Troubleshooting Using Kernel Diagnostic Tests later in this section to determine failure and recommended repair action.

The test loops until the problem is repaired (with the exception of the floppy test which will not loop if a hard disk is installed).

Table 8-2 summarizes the MPU kernel fault codes that can be displayed by the diagnostic LEDs if a kernel diagnostic test fails. Figure 8-3 lists miscellaneous LED codes that could be displayed during the boot process.

Table 8-2
Diagnostic LED Fault Code Summary

LED Code		Description
MSB	LSB	
0000	0000	Initial value displayed at start of power-on sequence
0000 0000	0001 000F	Start ROM complimentary word test Failed ROM complimentary word test
0000 0000	0010 00F0	Start ROM checksum even compare Failed ROM checksum even compare
0000 0000	0011 00FF	Start ROM checksum odd compare Failed ROM checksum odd compare
0000 0000	0100 bbbb	Start ROM checksum odd compare Failed ROM checksum odd compare bbbb = bit number in error 0000 = low bit, i.e., bit 0 0001 = next bit, i.e., bit 1 1111 = high bit, i.e., bit 15
0000 0000	0101 0F0F	Start RAM address independence test Failed RAM address independence test
0000	0110	Start vector table move
0000 0000	0111 0FFF	Floppy interrupt test Failed floppy interrupt test
0000 0000	1000 F000	Video interrupt test Failed video interrupt test
0000 0000	1001 F00F	Start floppy disk track register check (floppy test) Failed floppy disk track register check
0000 0000	1010 F0F0	Start floppy disk sector register check ($AA) Failed floppy disk sector register check ($AA)
0000 0000	1011 F0FF	Start ST506/412 hard disk sector count register test Failed ST506/412 hard disk sector count register test
0000 0000	1100 FF00	Start ST506/412 hard disk sector number register test Failed ST506/412 hard disk sector number register test
0000 0000	1101 FF0F	Start ST506/412 hard disk cylinder low test Failed ST506/412 hard disk cylinder low test
0000 0000	1110 FFF0	Start ST506/412 hard disk cylinder high test Failed ST506/412 hard disk cylinder high test
0000 0000	1111 FFFF	Start ST506/412 hard disk SDH register test Failed ST506/412 hard disk SDH register test
0001 000F	0000 0000	Start ST506/412 hard disk memory test Failed ST506/412 hard disk memory test
0000 0000	1011 F0FF	Intiate IDE hard disk software reset Failed IDE hard disk software reset

Table 8-2
Diagnostic LED Fault Code Summary (Cont.)

LED Code		
MSB	LSB	Description
0000	1100	Intiate IDE hard disk internal diagnostics test
0000	FF00	Failed IDE hard disk internal diagnostics test
0000	FF0F	Failed IDE hard disk formatter device test
0000	FFF0	Failed IDE hard disk sector buffer test
0000	FFFF	Failed IDE hard disk ECC circuitry test
000F	0000	Failed IDE hard disk controlling microprocessor test
0001	0001	Start 2681 (RS232); set to disabled

(Cont.)

Refer to Table 8-3 for other LED codes that can be displayed during the boot process. These codes are presented for information purposes.

Table 8-3
Miscellaneous Boot Process LED Codes

LED Code		
MSB	LSB	Description
0001	0010	Enabling CPU for level 5*
0001	0011	Moving sio_cb to boot area
0001	0100	Starting restore drive A
0001	0101	Starting boot block read drive A
0001	0110	Booting A
0001	0111	Starting restore drive C
0001	1000	Starting boot block read drive C
0001	1001	Booting C
0001	1010	Calling booted code
0001	1011	Nothing found to boot: insert disk

**Processor is set to level 5 interrupt. All interrupt priorities that are level 5 and above are acknowledged.*

Troubleshooting Using Kernel Diagnostic Tests

If the power-on display (Figure 8-6) shows that a kernel test failed, locate the test in the following test descriptions and troubleshoot as described. If Kernel Diagnostic fails and there is no displayed message, read the MPU Diagnostic LEDs (as previously described), locate the test code in the following troubleshooting information, and troubleshoot as described. For example, if the diagnostic test sequence hangs and displays the message "

```
Failed the ROM Complimentary Test
```

Then troubleshoot according to information under probable cause and recommended action for failure of the *ROM Complimentary Word Test*.

NOTE

The left-most bit is the MSB; the right-most bit is the LSB.

The following tests are listed in the order they occur in the power-on sequence.

TEST FUNCTION: **Begin to Execute Boot Code**

LED CODE: **0000 0000**

DESCRIPTION: When the processor starts to execute ROM boot code, all LEDs are set to off (all LEDs are set on when power is initially applied), display RAM is cleared, and display controller circuits are set for display operation. At this time, the "Kernel Diagnostics Started" and related data is displayed on the monitor.

TEST FUNCTION: **Begin to Execute ROM Boot Code**

LED CODE: **0000 0001**

DESCRIPTION: Start ROM Complimentary Word Test. Checks that ROM data lines can be driven high and low. This is done by reading a word from ROM (80FFF8) , inverting the value read, and then comparing it to the next addressable word (80FFFA).

Probable Causes	Recommended Action
Wrong data in ROM or ROM failure	Replace even and/or odd ROMs. (MPU schematic 2)
CPU failure	Replace CPU. (MPU schematic 1)
Data or address bus failure	Check kernel data and address lines for shorts or opens.

TEST FUNCTION: **Failed the ROM Complimentary Word Test**

LED CODE: **0000 000F**

DESCRIPTION: Failed the ROM Complimentary Word test.

Probable Causes	Recommended Action
ROM failure	Suspect even and/or odd ROMs. (MPU schematic 2)

TEST FUNCTION: **Start ROM Checksum Even Compare Test**

LED CODE: **0000 0010**

DESCRIPTION: Starts the ROM Checksum Even Compare Test

Probable Causes	Recommended Action
ROM failure	Suspect even ROM. (MPU schematic 2)

TEST FUNCTION: **Failed ROM Checksum Even Compare Test**

LED CODE: **0000 00F0**

DESCRIPTION: Failed ROM Checksum Even Compare test. The even ROM failed to match the calculated checksum.

Probable Causes	Recommended Action
ROM failure	Suspect even ROM. (MPU schematic 2)

TEST FUNCTION: **Start ROM Checksum Odd Compare Test.**

LED CODE: **0000 0011**

DESCRIPTION: Starts the ROM Checksum Odd Compare test.

Probable Causes	Recommended Action
ROM failure	Suspect odd ROM. (MPU schematic 2)

TEST FUNCTION: **Failed ROM Checksum Odd Compare Test**

LED CODE: **0000 00FF**

DESCRIPTION: The odd ROM failed to match the calculated checksum.

Probable Causes	Recommended Action
ROM failure	Suspect odd ROM. (MPU schematic 2)

TEST FUNCTION: **Start RAM Data Independence Test**

LED CODE: **0000 0100**

DESCRIPTION: This subroutine tests the processor's RAM data bus for independence as follows:

1. For each long word in the RAM: set to $0000000.
2. For the first word in the RAM: the first location of RAM is checked to contain 0000.

   Each bit, one at a time, is asserted high and checked by reading the resultant word. For example: 0001 is written to RAM, then the same location is read to verify that it contains the value written. Next, 0002 is written and checked; then 0004, 0008, 0010, 0020, 0040, 0080, 0100, 0200, 0400, 0800, 1000, 2000, 4000, 8000. After each write, RAM is read and checked. If an error is detected, then the LED is set to match the failure. See Failure indication below.

Probable Causes	Recommended Action
Double bus fault	Connect a logic analyzer with PM 203 to MPU board. Start logic analyzer and Mainframe. Stop analyzer and examine data. (MPU schematics 1, 6 and 7)

TEST FUNCTION: **Failed the RAM Independence Test**

LED CODE: **0000 bbbb**

DESCRIPTION: Failed the RAM Independence test.

NOTE

***bbbb** = bit number in error (0000 = bit 0, 0001 = bit 1, ..., 1111 = bit 15). See explanation under 0000 0100 above.*

Probable Causes	Recommended Action
RAM data bit error	Determine which bit has failed by examining the LEDs. The LEDs labeled "bbbb" in the above descriptions indicate what bit failed. Refer to MPU schematics 6 and 7 to determine which RAM chip may have failed.

TEST FUNCTION: **Start RAM Address Independence Test**

LED CODE: **0000 0101**

DESCRIPTION: Start the RAM Address Independence test by performing the following:

1. For each long word in the block, set to $55555555.
2. For each short word in the block:
   - test for $55555555
   - set to $AAAAAAAA
   - test for $AAAAAAAA

   This test verifies the address decoding and the cell integrity of RAM. All long words in the block are left set to $AAAAAAAA.

Probable Causes	Recommended Action
Double bus fault	Connect a logic analyzer with PM 203 to MPU board. Start logic analyzer and Mainframe. Stop analyzer and examine data. (MPU schematics 1, 6 and 7)

TEST FUNCTION: **Failed RAM Address Independence Test**

LED CODE: **0000 0F0F**

DESCRIPTION: Failed RAM Address Independence test.

Probable Causes	Recommended Action
Bad RAM or address line	Press NMI to enter the Test Monitor. Run the RAM tests and examine the results (refer to description of *Test Monitor* at end of this section).

TEST FUNCTION: **Started the Flexible Disk Interrupt Test**

LED CODE: **0000 0111**

DESCRIPTION: Started the Flexible Disk Interrupt test. This routine executes the following sequence.

1. Disables all interrupts.
2. Tests if COMM pack is installed. If installed, disables COMM pack Interrupt.
3. Issues a clear force interrupt command to the flexible disk controller.
4. Issues a force interrupt command to the flexible disk controller.
5. Checks that flexible disk controller generated an interrupt.
6. Issues clear force interrupt command to the flexible disk controller.

Probable Causes	Recommended Action
No DTACK signal	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Failed Flexible Disk Interrupt Test**

LED CODE: **0000 0FFF**

DESCRIPTION: Failed Flexible Disk Interrupt test.

Probable Causes	Recommended Action
Interrupt not generated	Suspect flexible disk controller, WD1772. Check pin 2. (MPU schematic 10)
Interrupt multiplexer	Suspect interrupt multiplexer. (MPU schematic 8)
GLUE Gate Array	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Start No Interrupts Test**

LED CODE: **0000 1000**

DESCRIPTION: This test checks that there are no interrupts at the GLUE gate array.

Probable Causes	Recommended Action
No DTACK signal	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Failed No Interrupts Test**

LED CODE: **0000 F000**

DESCRIPTION: Failed No Interrupts test. The following bits are assigned to address 85F17E of the GLUE gate array:

Bit 0 = keyboard transmit
Bit 1 = keyboard receive
Bit 2 = level 2 (unused)
Bit 3 = hard disk
Bit 4 = 2681 (DUART) IRQ
Bit 5 = COMM pack
Bit 6 = RS-232C transmit (rear panel)
Bit 7 = RS-232C receive (rear panel)
Bit 8 = display (video) gate array
Bit 9 = TekLink gate array
Bit 10 = flexible disk controller IRQ
Bit 11 = clock tick
Bit 12 = Level 6 (unused)
Bit 13 = flexible disk controller DRQ
Bit 14 = NMI
Bit 15 = power failure

Probable Causes	Recommended Action
Video gate array	Suspect Video gate array. (MPU schematic 14)
Interrupt multiplexer	Suspect interrupt multiplexer. (MPU schematic 8)
GLUE Gate Array	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Start Flexible Disk Track Register Test**

LED CODE: **0000 1001**

DESCRIPTION: Checks that the track register can be written to and read from (write 0, test for 0). It checks that all track register bits can be written and read (the value $01, then $02, ..., $08 is written to and then read from the track register to verify that each bit can be independently set).

Probable Causes	Recommended Action
No DTACK signal	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Failed Flexible Disk Track Register Test**

LED CODE: **0000 F00F**

DESCRIPTION: Failed Flexible Disk Track Register test (for data independence).

Probable Causes	Recommended Action
Data lines shorted or open	Check data lines to WD1772 and from floppy disk control latch. (MPU schematic 10)
Flexible Disk Controller	Suspect WD1772 or floppy disk control latch. (MPU schematic 10).

TEST FUNCTION: **Start Flexible Disk Sector Register Check**

LED CODE: **0000 1010**

DESCRIPTION: First, checks that the Sector Register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Causes	Recommended Action
No DTACK signal	Suspect GLUE gate array. (MPU schematic 5)

TEST FUNCTION: **Failed Flexible Disk Sector Register Check**

LED CODE: **0000 F0F0**

DESCRIPTION: Failed Flexible Disk Sector Register Check.

Probable Causes	Recommended Action
Flexible disk controller	Suspect WD1772 or floppy disk control latch. (MPU schematic 10)

TEST FUNCTION: **Start ST506/412 Hard Disk Sector Count Register Test**

LED CODE: **0000 1011**

DESCRIPTION: Checks that the sector count register can be written and read (write 0, read 0). Checks that all sector count register bits can be written and read. The value $01, the $02, ..., $80 is written to, then read from the sector count register to verify that each bit can be independently set.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic in applicable mainframe service manual).

TEST FUNCTION: **Failed ST506/412 Hard Disk Sector Counter Register Test**

LED CODE: **0000 F0FF**

DESCRIPTION: Failed ST506/412 Hard Disk Sector Count Register test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
Data buffers	Suspect data buffers on Hard Disk Controller board (refer to HDC schematic 3 in the applicable mainframe service manual).
Hard Disk Controller	Suspect WD2010 (hard disk controller chip) on Hard Disk Controller board (refer to HDC schematic 4 in applicable mainframe service manual).

TEST FUNCTION: **Start ST506/412 Hard Disk Sector Number Test**

LED CODE: **0000 1100**

DESCRIPTION: First, checks that the sector register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic 1 in applicable mainframe service manual).

TEST FUNCTION: **Failed ST506/412 Hard Disk Sector Number Register Test**

LED CODE: **0000 FF00**

DESCRIPTION: Failed ST506/412 Hard Disk Sector Number Register test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (refer to HDC schematic 4 in applicable mainframe service manual).

TEST FUNCTION: **Start ST506/412 Hard Disk Cylinder Low Test**

LED CODE: **0000 1101**

DESCRIPTION: First checks that the Cylinder Low Register can be written with $AA, then checks that it can be written with $55.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic 1 in applicable mainframe service manual).

TEST FUNCTION: **Failed ST506/412 Hard Disk Cylinder Test**

LED CODE: **0000 FF0F**

DESCRIPTION: Failed ST506/412 Hard Disk Cylinder Low test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (Refer to HDC schematic 4 in applicable mainframe service manual).

TEST FUNCTION: **Start ST506/412 Hard Disk Cylinder High Test**

LED CODE: **0000 1110**

DESCRIPTION: First, checks that the Cylinder High Register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic 1 in applicable mainframe service manual)

TEST FUNCTION: **Failed the ST506/412 Hard Disk Cylinder High Test**

LED CODE: **0000 FFF0**

DESCRIPTION: Failed ST506/412 Hard Disk Cylinder High test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (Refer to HDC schematic 4 in applicable mainframe service manual).

TEST FUNCTION: **Start ST506/412 Hard Disk SDH Register Test**

LED CODE: **0000 1111**

DESCRIPTION: First, checks that the SDH register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic 1 in applicable mainframe service manual).

TEST FUNCTION: **Failed ST506/412 Hard Disk SDH Register Test**

LED CODE: **0000 FFFF**

DESCRIPTION: Failed ST506/412 Hard Disk SDH Register test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (Refer to schematic 4 in applicable mainframe service manual).

TEST FUNCTION: **Start the ST506/412 Hard Disk Memory Test**

LED CODE: **0001 0000**

DESCRIPTION: This test walks a bit across the ST506/412 hard disk memory as follows:

1. The hard disk memory address point is reset and 0001 is written.

NOTE

During read or write operations, the hard disk memory address point is incremented automatically.

2. Next, 0002 is written, followed by 0004, 0008, ..., 8000.
3. The hard disk memory address pointer is again reset and the memory is read and checked for errors.

Probable Causes	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC schematic 1 in applicable mainframe service manual).

TEST FUNCTION: **Failed ST506/412 Hard Disk Memory Test**

LED CODE: **000F 0000**

DESCRIPTION: Failed ST506/412 Hard Disk Memory test.

Probable Causes	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect schematic in the applicable mainframe service manual).
RAM	Suspect memory chips on Hard Disk Controller board (refer to HDC Schematic 2 in the applicable mainframe service manual).
Memory Address Pointers	Suspect RAM address counter on Hard Disk Controller board (refer to HDC Schematic 1 and 6 in the applicable mainframe service manual).

TEST FUNCTION: **Initiate IDE Hard Disk Software Reset**

LED CODE: **0001 1011**

DESCRIPTION: Reset the IDE hard disk drive to a known state.

Probable Causes	Recommended Action
No BTACK signal	Suspect U451, decoding PAL, on IDE Interface board.

TEST FUNCTION: **Failed IDE Hard Disk Software Reset**

LED CODE: **0001 F0FF**

DESCRIPTION: The IDE hard disk drive failed software reset test.

Probable Causes	Recommended Action
IDE hard disk drive	Replace the IDE hard disk drive.

TEST FUNCTION: **Initiate IDE Hard Disk Internal Diagnostics Test**

LED CODE: **0000 1100**

DESCRIPTION: This test issues a command to the IDE hard disk drive to start the internal diagnostics test of the hard disk drive circuitry.

Probable Causes	Recommended Action
No _BTACK signal	Suspect U451, decoding PAL, on IDE Interface board.

TEST FUNCTION: **Failed IDE Hard Disk Internal Diagnostics Test**

LED CODE:
0000 FF00 (Failed IDE hard disk internal diagnostics test.)
0000 FF0F (Failed IDE hard disk formatter device test.)
0000 FFF0 (Failed IDE hard disk sector butter test.)
0000 FFFF (Failed IDE hard disk ECC circuitry test.)
000F 0000 (Failed IDE hard disk control microprocessor test.)

DESCRIPTION: Failed IDE hard disk internal diagnostics test. The LED code indicates the part of the hard disk circuitry that failed.

Probable Causes	Recommended Action
IDE hard disk drive	Replace the IDE hard disk drive.

TEST FUNCTION: **Start RS-232-C (DUART 2681) and Set to Disable Test**

LED CODE: **0001 0001**

DESCRIPTION: Start RS232 (DUART 2681) and Set to Disable test.

Probable Causes	Recommended Action
No DTACK signal	Suspect GLUE gate array (refer to MPU schematic 5).

Test Monitor "Trap" Codes

ROM code contains a test monitor that can be used for low-level debugging of the MPU kernel circuitry. Several of the ROM-based tests can have errors that will be "trapped" to the test monitor. This condition is indicated by the following codes:

0Fxx xxxx	entered test monitor awaiting input from 1200C01 COMM pack
F0xx xxxx	entered test monitor awaiting input from read panel RS-232C port

Refer to the *Kernel Test Monitor* description in Appendix A for further information regarding the use of this monitor.

Section 9
SYSTEM DIAGNOSTIC SOFTWARE

INTRODUCTION

This section describes how to use System Diagnostic Software and provides a detailed description of each diagnostic test.

System Diagnostic Software is a structured set of test routines used for hardware verification and troubleshooting. These tests are located on the System Diagnostics disk shipped with each PRISM 3000 or 2500 TestLab mainframe. (Some PRISM 3000 Systems may have diagnostics loaded into a DIAGS file on the hard disk.) All tests for the MPU board and associated peripheral modules are described in this section. (Diagnostic software for acquisition modules is described in separate acquisition module service manuals.) This section contains the following:

- Definition of diagnostic terms
- Diagnostics structure
- Standard and optional diagnostic software
- Using diagnostic software
- Test descriptions

Definition of Diagnostic Terms

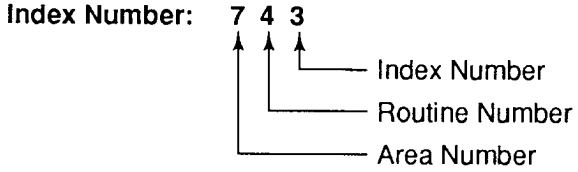
The following provides a brief description of diagnostic terms:

Module. The highest level of diagnostics. A *module* is the highest level to which a fault can be repaired. Most customer-site repairs are made at this level.

Area. An electrical *module* may have several functional *areas* (circuits) that need testing. Once you know the specific fault area, you can chose specific tests for lower-level troubleshooting.

Routine. A *routine* tests a specific circuit or function "inside" an area.

Index Information. *Index* information provides component-level information about the specific test routine that failed. In most cases, Index information directs you to the most-likely failed component, signal path, or connector pin. Most routines contain one or more indices. The following defines the numerical significance of an index number:



Detailed troubleshooting information for the indicated index is included as part of the test descriptions provided later in this section. As shown in the example, the numeral "3" indicates the third "index" of the failed test. To troubleshoot, simply refer to the test description for the failed test, locate the index number "3," and troubleshoot the failure as described.

DIAGNOSTICS STRUCTURE

Introduction

Table 9-1 lists the diagnostic routines provided on the PRISM 3000 (or 2500 TestLab) System Diagnostic disk. (Diagnostic routines for acquisition modules are described in separate acquisition module service manuals.) Not all tests listed in Table 9-1 are available for a particular mainframe product. However, all tests are listed here to aid your understanding of how diagnostics are configured, and to show which tests are standard and optional for a particular mainframe product.

Diagnostic Configuration

Individual tests are grouped to enable a technician to quickly and easily locate a test area or a specific test to run for a particular malfunction, or suspected malfunction. Table 9-1 and Figure 9-1 show that MPU Module diagnostic software consists of test modules for the CPU, Hard Disk, and COMM Pack. Test modules consist of one or more test areas. Test areas consist of one or more individual test routines. Individual routines test specific circuits or functions within a test area.

A test routine may have one or more index numbers to better indicate the specific sequence within a routine that failed. For example, Figure 9-1 shows the diagnostic routines for the RS-232C area of the CPU (MPU board) module. Note that it shows four index numbers. By noting the index number of a failed test, you can then refer to the detailed test description (later in this section) for component-level testing and repair instructions. Diagnostic tests for other modules are organized in a similar manner.

NOTE

The letter "M" preceding a test name identifies that test as a "manual test." Manual tests require user interaction and/or special test fixtures to be exercised.

Table 9-1 also shows the routines that run automatically as part of a RUN ALL (or LOOP ALL) modules sequence. Refer to *Using Diagnostic Software* for more information. As stated earlier, manual tests require user interaction and/or special test fixtures to be exercised.

Table 9-1
Diagnostic Software

Module	Area	Routine No.	Routine Name	Description	Auto Seq.
CPU (MPU Board)	ROM	0	Even ROM	Performs Checksum test on Even ROM.	X
		1	Odd ROM	Performs Checksum test on Odd ROM.	X
	Keyboard	0	Stuck key	Tests for stuck keys on Keyboard/ Console.	X
	Clock	0	Clock Registers	Checks read/write registers and checks for bad data lines.	X
		1	Clock Counter	Checks clock calendar hundreds register.	X
		2	Clock Rollover	Checks that all clock times will roll to minimum value.	X
	RS232	0	DUART existence	Verifies that host channel exists and can be accessed.	X
		1	Keyboard Internal Loopback	Internally transmits a character string to channel A.	X
		2	Host Internal Loopback	Internally transmits a character string to channel B.	X
		3	Host External Loopback	Performs external loopback test. Requires external loop back connector. **NOTE**: Test runs without connector, but will fail.	X
	Glue Gate Array	0	Glue Register	Writes pattern to Glue read/ write registers and reads back.	X
		1	Glue Interrupt	Sets and checks 13 kernel interrupt signals.	X
		2	Beeper	Checks beeper (audio) circuit.	X
	Floppy Disk	0	Floppy existence	Checks that floppy controller is accessible.	X
		1	Floppy ready	Tests that drive is spinning and ready for read/write functions.	X
		2	Floppy motor	Tests the Motor On signal from floppy controller.	X
		3	Floppy track 0	Tests that TR_0 signal goes low when head is at Track 0.	X
		4	Floppy read	Checks that read is performed on side 0.	X

(Cont.)

Table 9-1
Diagnostic Software (Cont.)

Module	Area	Routine No.	Routine Name	Description	Auto Seq.
CPU (MPU Board) (Cont.)	Tek Com	0	Register	Writes four patterns to gate array registers.	X
		1	Immediate Read	Tests tri-state outputs and then loops data out and back in.	X
		2	Interrupt	Test immediate write and acquisition module interrupt.	X
		3	RAM	Tests data and address independence and RAM cell integrity.	X
		4	Buffer Transfer	Tests transfer of data between A and B buffers.	X
		5	TekEvent	Tests each SIGNAL[1:4} line (not part of TestLab diagnostics software).	X
	Video	0	RAM	Tests RAM and gate array.	X
		1	Video Array	Sets Video GA to test windowing, screen readback, and drawing engine.	X
	Set Time	M	Set Time/Date	Allows manual setting of day, month, and time.	
	Manual Keyboard	M	Manual Keyboard	Allows manual check of all keyboard/console keys	
	Manual Floppy	0	Floppy Disk Change	Tests operation of DISK_CHNG signal. Requires scratch disk.	
		1	Floppy Read/ Write	Writes to first sector of each track and reads back. Requires scratch disk.	
		2	Floppy Alignment	Uses Dysan Diagnostic disk to check alignment, centering and spindle speed	
	Manual Display	0	Display	Test operation of display controller by driving monitor with test patterns. Checks all display types.	
	Manual Clock	0	Clock Adjust	Used to adjust Clock oscillator. Refer to *Adjustment Procedures* in Section 5.	
	Manual Module ID	M	Module ID	Used as aid for troubleshooting when there is problem identifying module.	

(Cont.)

Table 9-1
Diagnostic Software (Cont.)

Module	Area	Routine No.	Routine Name	Description	Auto Seq.
Hard Disk Drive (Only runs when Hard Disk is installed)	Hard Disk Memory and Controller for ST506/412-interface drive	0	Registers	Checks controller registers in the hard disk controller IC	X
		1	Data Line Independence	Checks data lines, DC[0:15] and associated circuitry.	X
		2	Address Line Independence	Checks address counter, address lines AC[0:12], and associated circuitry.	X
		3	RAM Integrity	Tests the integrity of RAM and associated circuitry.	X
		4	Read/Write	Writes 1 Kbyte file to hard disk then reads file.	X
	Hard Disk Format for ST506/412-interface drive	M	Format	Formats ST506/412-interface hard disk drive.	
	Hard Disk Diagnostics for IDE-interface drive	0	HD Diagnostics	Verifies proper operation of the formatter device, sector buffer, ECC circuitry, and control microprocessor for the IDE-interface hard disk drive.	X
	Hard Disk Format for IDE-interface drive	M	HD Format	Formats IDE-interface hard disk drive.	
1200C01 (Only runs when 1200C01 is installed)	RS232	0	UART Internal Loop	Performs internal loopback test by internally transmitting data string.	X
		1	Host External Loopback	Performs external loopback test. Requires external loop back connector. **NOTE**: Test runs without connector, but will fail.	X

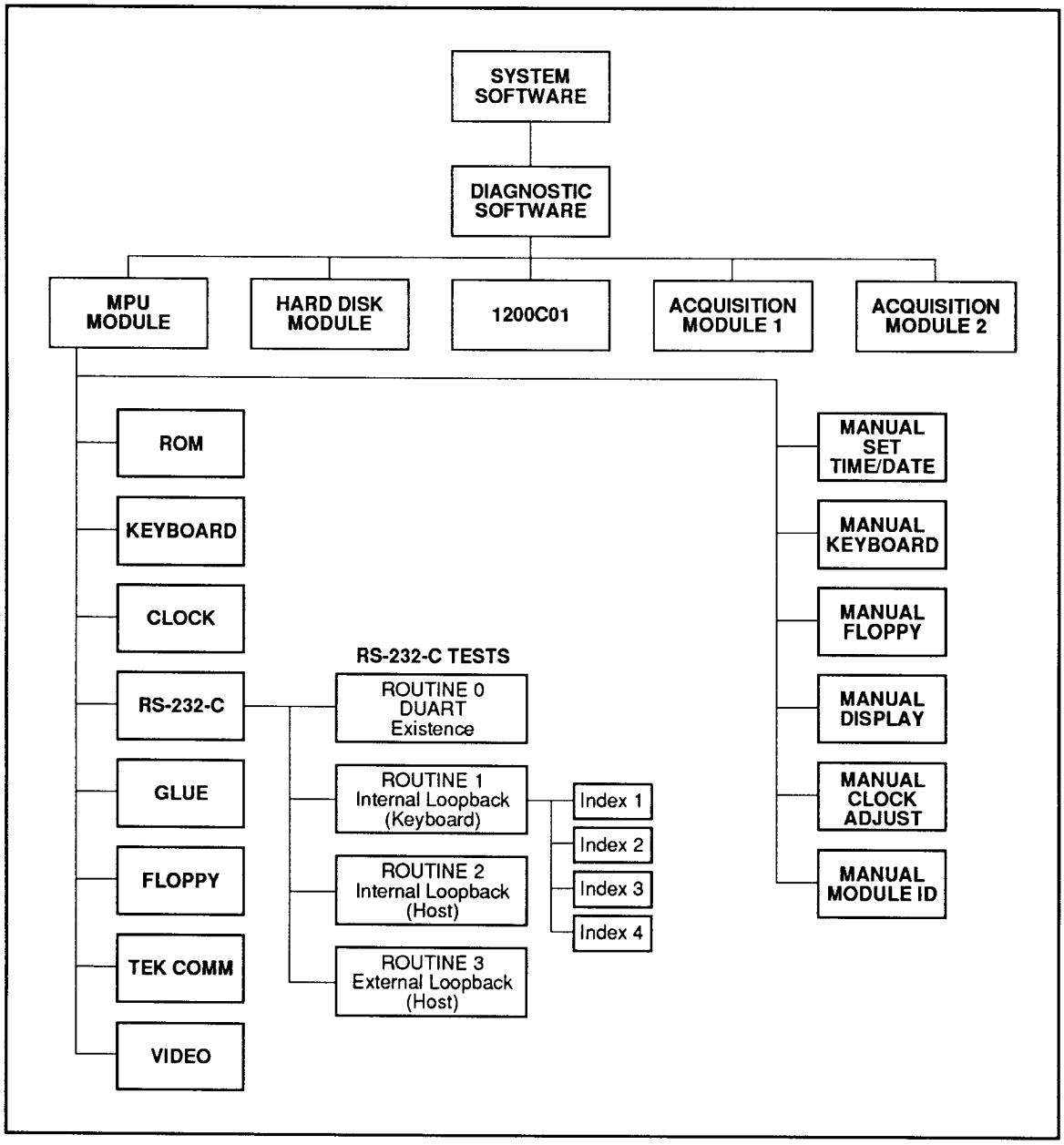


Figure 9-1. Structure of diagnostic software.

Disk Media

The floppy disk is the standard media for System Diagnostic Software. The PRISM 3000 Extended Diagnostic Software is also provided on a floppy disk. (Refer back to *Standard and Optional Diagnostic Software* for additional information.) The PRISM 3000 products can have all diagnostics software (standard and extended diagnostic tests) loaded onto the optional Hard Disk module. The 2500 TestLab products have diagnostic software configured only on a separate floppy disk. Refer to *Loading Diagnostics Software* later in this section for detailed information on this subject.

Diagnostic Configuration Error Indexes

After the Diagnostic is loaded into RAM, it checks the system configuration table to determine the ports and acquisition modules installed in the system. The Diagnostic Monitor then checks to ensure that diagnostic files are available to run diagnostics on the system modules.

Diagnostic configuration errors occur when files in the Diagnostic Directory are either non-existent or are corrupted. Errors can also occur if the operating system software is corrupted.

NOTE

Use the NOTES key whenever you need a quick information summary about the current state of system operation.

A configuration error index consists of a three-digit number displayed on the error line (top character line) of the display. More than one three-digit error index can be displayed. How many error indexes are displayed depends on the number of configuration errors detected by the Diagnostic Monitor. The following describes how to interpret an error index.

Interpret the error index as follows:

Digit three identifies the diagnostic configuration error to either a hardware port or an acquisition module. For example, if the third digit is. . .

0, then a COMM Pack or hard disk port configuration problem occurred.

1, then an acquisition module configuration problem occurred.

Digit two identifies the specific port or module associated with the configuration error. For example, if digit three is 0 and the digit two is. . .

0, then the error is associated with COMM Pack port.

1, then the error is associated with Port 3 (there is currently no hardware associated with this port).

2, then the error is associated with the hard disk port.

If **digit three is** 1 and **digit two** is:

0, then error is associated with internal acquisition module #0.

1, then error is associated with internal acquisition module #1.

2, then error is associated with internal acquisition module #2.

3, then error is associated with internal acquisition module #3.

4, then error is associated with internal acquisition module #4.

5, then error is associated with internal acquisition module #5.

6, then error is associated with internal acquisition module #6.

7, then error is associated with internal acquisition module #7.

8, then error is associated with external acquisition module #8.

8, then error is associated with external acquisition module #9.

A, then error is associated with external acquisition module #A.

B, then error is associated with external acquisition module #B.

C, then error is associated with external acquisition module #C.

D, then error is associated with external acquisition module #D.

E, then error is associated with external acquisition module #E.

F, then error is associated with external acquisition module #F.

Digit one identifies the specific error that occurred for the port or the acquisition module. If digit one is. . .

1, then failed fingerXchg to ZEKZ [FingerXchg( ) returns the exchange ID (XID) of a process.]

2, then failed toXchg to ZEKZ [toXchg( ) send a message to a process].

3, then failed to load file [ZEKZ could not load file].

4, then error in dev_table [dev_table has unknown value, dev_id_tbl empty].

5, then failed fingerXchg to GA_Z [fingerXchg( ) returns the exchange ID (XID) of a process]

6, then failed toXchg to GA_Z [toXchg( ) send a mail message to a process].

7, then failed to track file [GA_Z could not track file loaded by ZEKZ]

8, then error in card_tbl [card_tbl has unknown value, card_id_tbl empty]

9, then DIAG header error [module record could not be added to monitor's module_record_List because Diag header has unknown value; must contain DIAG_VALIDATION]

A, then failed to allocMem [a "no memory" was available when trying to copy diagnostic data structures from a previously loaded diagnostic module. This error should only occur when two or more of the same acquisition modules are installed in the system.]

USING DIAGNOSTIC SOFTWARE

Diagnostic software is easy to use. User information is provided as follows:

- Required equipment
- Diagnostic menu
- Loading diagnostics software–PRISM 3000 systems
- Loading diagnostics software–2500 TestLab systems
- Manually exercising diagnostic tests
- Interpreting pass/fail indications
- Notes information
- Using diagnostics for system verification
- Using diagnostics for troubleshooting

Required Equipment

In order to exercise diagnostic tests on the System Diagnostics Software Disk you need the following:

1. Mainframe with MPU board, display monitor, keyboard, and disk drive
2. PRISM 3000 System Diagnostic Disk (Tektronix part number 063-0165-XX)
   TestLab System Diagnostic Disk (Tektronix part number 062-9925-XX)
3. External RS-232C loopback connector (Tektronix part number 013-0173-01)
4. DYSAN® Digital Diagnostic Diskette Model 305-400 (Vendor number 810244)

The Diagnostic Menu

When Diagnostic mode is entered, a menu similar to the one shown in Figure 9-2 is displayed. Note how it resembles the diagnostic structure shown in Figure 9-1. The menu shows all installed diagnostic modules, test areas for the selected diagnostic module, tests for the selected area, and index numbers for the selected tests.

NOTE

Note the area tests preceded by the letter "M." The letter 'M" indicates that the operator must perform manual interaction in order to run the test. For example, the "Set Time/Date" routine requires that the user manually input date and time information.

Each module and area that fails is shown on the diagnostic menu with a failure indication. Each routine that fails shows the failure address, expected data, and the actual data, along with an error index. Refer to *Interpreting Pass/Fail Indications* later in this section for additional information.

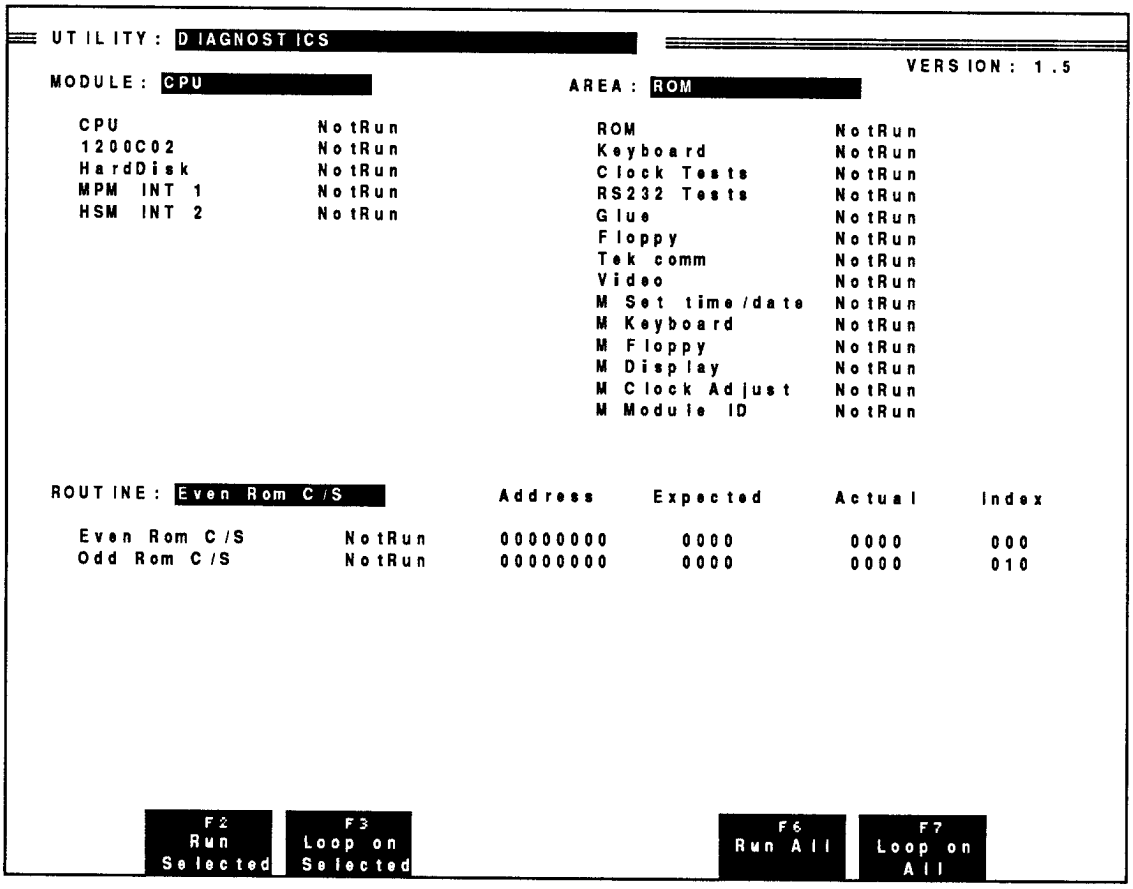


Figure 9-2. Diagnostic Menu.

Loading Diagnostics Software–PRISM 3000 Systems

The PRISM 3000 systems have three ways to load diagnostics software:

1. You can add diagnostics to your system disk so that they automatically load and run during the power-on sequence.
2. You can put diagnostics on you system disk in a DIAG directory so they are more easily available for loading.
3. You can keep diagnostics on a separate disk (or in a nonautoloading directory) and load them manually whenever you want to run a system test.

To successfully power on, there must be a file named DIAGS in the BOOT directory on the PRISM system disk. If this file is the same as the file DIAG_STB from the diagnostics floppy disk, no diagnostics (except for the ROM-based kernel tests) are run during the power-on process. If the DIAGS file is the same as the file DIAG_MAN from the System Diagnostics floppy disk, diagnostics are run automatically during the power-on sequence.

Running Diagnostics Automatically at Power-On

To configure your system disk to run diagnostics automatically during the power-on process, do the following (refer to Section 6 of the *PRISM 3002 System User's manual* for instructions on copying files and creating directories):

1. Use the Copy File operation in the Disk Services menu to copy the file DIAG_MAN from your System Diagnostics floppy disk into a file called DIAGS in the BOOT directory on your system disk.
2. Create a directory called DIAG on your system disk, if it does not already exist.
3. Copy all the files (other than DIAG_MAN) from the DIAG directories on your diagnostic floppy disk and on your application module disk into the DIAG directory on your system disk.
4. If you are using a floppy disk as your system disk, remove it from the floppy disk drive.
5. Turn off your mainframe, wait a few seconds, then turn it on again. If you are using a floppy disk as your system disk, insert it into the floppy disk drive.

NOTE

Do not press any keys during the power-on sequence; this will cause a diagnostic keyboard failure to occur.

Diagnostics software gets loaded as needed from the DIAG directory. If you are using diagnostics on a floppy disk, leave the disk installed in the drive until all diagnostics tests are complete.

When the system is powered on with diagnostics in the BOOT directory, the diagnostics run automatically during the power-on sequence. The mainframe first runs Compute Kernel Diagnostics, after which the system software is loaded and testing continues with selected system tests that verify the functionality of other MPU board hardware, keyboard, floppy disk drive, color monitor, flat panel display, hard disk controller, and hard disk drive.

NOTE

If you do not want to automatically load and run diagnostic software when powering on the mainframe, complete Manually Loading and Running Diagnostics *in this section.*

If a diagnostics failure occurs, a diagnostic screen will remain displayed, indicating which test failed.

Manually Loading and Running Diagnostics

To configure your system disk for convenient manually loading of diagnostics, do the following (Refer to your applicable system user's manual for instructions on copying files and creating directories):

1. Use the Copy File operation in the Disk Services menu to copy the file DIAG_STB from your diagnostics floppy disk into a file called DIAGS in the BOOT directory on your system disk.
2. Create a directory called DIAG on your disk, if it does not already exist. If you have a hard disk, create the DIAG directory on it. If you are using only floppy disks, you can either put the DIAG directory on the system disk or on a floppy disk just for diagnostics.
3. Copy all the files (including DIAG_STB) from the DIAG Directories on your diagnostic floppy disk and on your application module disks into the DIAG directory on your disk.
4. Now, when you wish to manually load diagnostics, use the Load Application operation in the Save/Restore menu to load the file DIAG_MAN into the SYSTEM module. Detailed instructions are:
   a. Access the Save/Restore menu by pressing Util, then scroll through the menus until the Save/Restore menu is selected.
   b. In the operation portion of the Save/Restore menu, select Load Application as the operation.
   c. Fill in the parameter portion of the Save/Restore menu as follows:

      Source Disk. Select the disk (floppy or hard) from which you want to load diagnostics.

      Source Directory. Select DIAG since this is the directory that contains diagnostic software.

      Source File. Select DIAG_MAN since this is the file that contains diagnostic monitor software.

Destination Module. Select SYSTEM since you want to load diagnostics into RAM allocated to the MPU board.

d. Press F1 to load diagnostics. A message on the top line of the display tells you when the load operation is complete.

5. Your system is now configured so that you can manually exercise diagnostics tests.

Loading Diagnostics Software–2500 TestLab Systems

System Diagnostics Software for the 2500 TestLab products cannot be loaded onto a System disk. These products automatically load and exercise diagnostics software at power-up when the System Diagnostics disk has been inserted into the floppy drive in place of the 2500 System floppy disk. The 2500 TestLab then remains in Diagnostics mode for manual exercising of individual tests.

To exit a 2500 TestLab mainframe from the Diagnostics mode you must eject the 2500 System Diagnostics disk, and then boot the system from either the hard disk drive or System Software floppy disk.

Manually Exercising Diagnostic Tests

To manually exercise diagnostics software, you must manually enter diagnostics mode, as previously explained.

When the Diagnostics menu is displayed you can then exercise a diagnostic test or a set of tests by first selecting the test or test sequence, then pressing the appropriate Special Function key to initiate the test or test sequence. Proceed as follows:

1. Determine whether you want to run a specific routine, or sequence of routines (test area or test module).
2. Move the cursor to select the desired test or test sequence.
   - Use the cursor position keys to move the cursor from one menu field to another. Or, use the NEXT key to move to the next field, the PREVIOUS key to move to the previous field, the HOME key to move the cursor to the utility (menu select field) in the upper left corner of the menu.
   - Use the KNOB or the SELECT key to select a specific module, area, or routine.

NOTE

When you select a module, all test areas for the module are displayed as well as all the test routines for the first area of the test module.

3. Activate the test by pressing the desired Function Key.

Function Key Explanation

Use the Special Function Keys to exercise the selected test or sequence of tests. The diagnostic menu displays the active function keys on the bottom of the menu. Diagnostic software indicates current test activity by reversing the video of the selected key(s). These keys are assigned functions as follows:

F1 **STOP.** Stops the selected test activity. The F1 is displayed on the menu after the activation of a test or test sequence.

F2 **RUN SELECTED.** Runs the selected routine, the selected area tests, or the selected module tests.

F3 **LOOP ON SELECTED.** Continuously loops on the selected test, the selected area tests, or the selected module tests. Press the STOP key to break the loop.

F6 **RUN All.** Runs all test routines, all area tests, or all module tests depending on where the cursor is placed on the diagnostic menu. For example: all tests for all modules are run when the cursor is located in the modules field; all areas for the selected module are run when the cursor is located in the area field; and all routines of a specific area are run when the cursor is located in the routine field.

F7 **LOOP ON ALL.** Loops on all test routines, all area tests, or all module tests depending on where the cursor is placed on the diagnostic menu. For example: all tests for all modules are continuously looped when the cursor is located in the modules field; all areas for the selected module are continuously looped when the cursor is located in the area field; and all routines of a specific area are continuously looped when the cursor is located in the routine field.

Interpreting Pass/Fail Indications

When a test is run, the Diagnostic Menu gives pass/fail information. For example, assume that you are running all tests for all modules and that there were several failures.

First, the diagnostic software cycles through all tests for all modules (refer to Table 9-1 for tests that can be exercised in an auto sequence). As the software exercises the tests in sequence, it notes pass/fail status. If a test fails, the software retains failure (index) information, then continues with the next test in sequence.

After all tests in the sequence are exercised, the software displays the first test, of the first area, of the first module that failed. You can obtain failure information on other modules by selecting through the modules and areas as previously described.

Notes Information

On-line (NOTES) documentation is available for each selection; module, area, routine, and index. This explanatory information can be accessed by pressing the NOTES key. Detailed information on each error index is located under *Index* information provided with each detailed routine description later in this section.

Using Diagnostics for System Verification

Diagnostics are designed to help verify the operation of the MPU board and associated modules. The successful completion of all diagnostic tests verifies the operational integrity of these modules. Also, any installed acquisition modules will be supported with related module diagnostics. (Diagnostic software for acquisition modules is described in acquisition module service manuals.) Thus, complete system verification can be obtained by exercising all diagnostic tests for all modules.

Complete system verification should be done following module replacement/repair or as part of an incoming acceptance inspection.

The procedure is as follows:

1. Load Diagnostic Software.
2. When the Diagnostic Menu is displayed, position the cursor to the module field of the diagnostic menu.
3. Press the RUN ALL (F6) Special Function Key. This initiates the running of all the tests for all the modules installed in the system. Testing will continue until all the tests for all the modules have been run, or you press the STOP (F1) Special Function Key.
4. The successful completion of all tests for all modules verifies system functionality. If a test fails, refer to *Troubleshooting Using System Diagnostics* below.

NOTE

RUN ALL will not run areas that have an "M" preceding the area name. These tests must be manually selected and run.

Using Diagnostics for Troubleshooting

Diagnostic tests support troubleshooting to the module- and component-levels.

Module-Level Diagnostics.

Sequencing all module diagnostics (as described in *Using Diagnostics for System Verification)* provides reasonable assurance that the MPU board and associated peripherals are functional. When performing customer-site repair, replace the indicated bad module, cycle power, and run the system verification sequence as previously described.

NOTE

After replacing a module, it is recommended that you exercise all module tests (including manual diagnostic routines) to provide more complete performance verification of the replaced module in the system environment.

Component-Level Diagnostics.

Diagnostic tests support troubleshooting and repair of the MPU board to the component level. (Refer to the applicable acquisition module service manuals for related component-level diagnostic tests.)

The fault isolation capability of the Diagnostic routines can usually identify circuit failures to five parts LSI or one part VLSI. Thus, diagnostic software, coupled with the use of module theory, circuit schematics, component location drawings, etc., can help a technician efficiently locate and repair circuit failures at the component level.

Fault isolation and repair of a known bad module can be efficiently performed by following the general troubleshooting procedures outlined below.

1. With the known bad module installed, cycle power then load diagnostic software.
2. Move the cursor to the module field and select the known bad module using either the KNOB or the SELECT key.
3. Press the desired Function Key (F6 or F7) to exercise tests for the selected module.
4. Note the pass/fail indications in the module, area, and routine fields. Note especially the index number(s) displayed for any failed routines.
5. Use the NOTES key to obtain abbreviated troubleshooting information on the failed area and routine.
6. Note the "expected" and "actual" data and the index number following the failed routine. Locate troubleshooting information for a particular index number in the detailed test description located later in this section.
7. If additional information is needed, refer to the MPU board theory, schematics, component location drawing, etc., elsewhere in this manual.
8. At this point, you can attach test equipment at key circuit points on the module and then exercise the failed routine (or area) using LOOP ON SELECTED for intermittent failures, and RUN SELECTED for hard failures.

NOTE

Figure 3-1 shows a diagnostic test trigger test point (J390) on the MPU board. A trigger signal is applied to this test test point each time a diagnostic test is initiated (excluding kernel diagnostic tests that are exercised as part of the boot process).

9. Make the necessary repairs then cycle power and run the complete set of tests for the module to verify repair.
10. Repeat Steps 2-9 for any other failures.

This completes the instructions for using System Diagnostics.

TEST DESCRIPTIONS

The following is a detailed description of the tests associated with the MPU board module, the Hard Disk module, and the 1200C01 COMM Pack Module.

NOTE

Descriptions of diagnostic tests for acquisition modules are located in their respective service manuals.

The following detailed test and index descriptions are summarized in on-line documentation displays. You access the Documentation displays by pressing the NOTES key when in System Diagnostics mode.

MPU Module Test Descriptions

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU Board) Module, Manual Floppy Area, and test Routine 2 are selected. If you enter Diagnostic Mode and select the MPU module, you will see the MPU circuit areas that are tested. Test descriptions are presented here in the order as listed on the display. Refer to Section 4, *Theory of Operation*, for a detailed description of the MPU board circuits The MPU module consists of the following test areas:

- ROM
- Keyboard
- Clock
- RS-232C
- GLUE
- Floppy
- Tek Comm (TekLink Interface)
- Video
- Manual Set Time/Date
- Manual Keyboard
- Manual Floppy
- Manual Display
- Manual Clock Adjust
- Manual Module ID

TEST AREA: ROM

Circuit Overview

The MPU Board Schematic Sheet 2 shows the ROM circuits. Read Only Memory consists of two 256 Kbyte erasable/programmable read only memory chips. One chip stores the odd-addressed byte KD[00:07]; the other chip stores the even-addressed byte KD[08:15]. These 32K by 8-bit ROMs store the instructions for the power-up process and for loading the operating system from the system disk.

Rom Area Tests

The MPU Board ROM is tested using the following diagnostic routines:

- Even ROM test
- Odd ROM test

Routine 0: **EVEN ROM TEST**

Description: This routine performs a checksum on the even ROM that stores bits KD[00:07]. The calculated checksum is then compared to the checksum stored in the ROM trailer.

Algorithm: The first checksum byte = address _prt(A1).

1. Odd checksum:
    a. Add byte to losum(D1) preset A1 = odd address
    b. Add any carry to oddlosum(D1)
    c. Add losum(D1) to oddhisum(D2)
    d. Add any carry to oddhisum(D2)
2. Even checksum:
    a. Decrement address (A1) = even address
    b. Add any carry to evenlosum(D3)
    c. Add losum(D1) to evenhisum(D4)
    d. Add any carry to evenhisum(D4;
    else put the odd checksum into the high word of D0 and the even checksum into the low word of DO and return.
3. Return:
    a. Hibyte DO = odd ROM checksum
    b. Lobyte DO = even ROM checksum

Path Tested: Even ROM (U410), kernel address lines KA[1:16], kernel data lines KD[00:07], and the ROM enable line.

Index 1: **Problem:** Even ROM failed checksum.

Actual = calculated checksum
Expected = checksum stored in the ROM trailer
Address = address in the ROM trailer where the checksum is stored.

Action: Check the address lines; check the data lines; check the ROM signal line. If these lines are OK, replace the even ROM, U410.

Routine 1: **ODD ROM TEST**

Description: This routine performs a checksum on the odd ROM that stores bits KD[08:15]. The calculated checksum is then compared to the checksum stored in the ROM trailer.

Algorithm: The first checksum byte = address _prt(A1).

1. Odd checksum:
    a. Add byte to losum(D1) preset A1 = odd address
    b. Add any carry to oddlosum(D1)
    c. Add losum(D1) to oddhisum(D2)
    d. Add any carry to oddhisum(D2)
2. Even checksum:
    a. Decrement address (A1) = even address
    b. Add any carry to evenlosum(D3)
    c. Add losum(D1) to evenhisum(D4)
    d. Add any carry to evenhisum(D4;
    else put the odd checksum into the high word of D0 and the even checksum into the low word of DO and return.
3. Return:
    a. Hibyte DO = odd ROM checksum
    b. Lobyte DO = even ROM checksum

Path Tested: Odd ROM (U415), kernel address lines KA[1:16], kernel data lines KD[08:15], and the ROM enable line.

Index 1: **Problem:** Odd ROM failed checksum.

Actual = calculated checksum
Expected = checksum stored in the ROM trailer
Address = address in the ROM trailer where the checksum is stored.

Action: Check the address lines; check the data lines; check the ROM signal line. If these lines are OK, replace the Even ROM, U410.

TEST AREA: KEYBOARD

Circuit Overview

The auto keyboard area consist of a single routine that tests for stuck keys on the keyboard and control console. It runs automatically at power-up, or it can be manually exercised.

Routine 0: **Keyboard Stuck Key Test**

Description: Checks of stuck keys and KNOB functions. If a key is stuck, this routine calls up the Manual Keyboard Test which then highlights the suspected stuck key.

Algorithm: The Stuck Key Test performs the following sequence.

1. Test for key input.
2. If key input detected, call up the Manual Keyboard test.
3. Test for KNOB input.
4. If knob input, call up the Manual Keyboard test.

Path Tested: Keyboard data path between keyboard and MPU board.

Index Refer to Index information for *Manual Keyboard Test.*

TEST AREA: CLOCK TESTS

Circuit Overview

Clock circuitry is shown on MPU Board Schematic Sheet 12. Calendar circuitry consists of the Signetics® ICM7170 clock calendar chip (U350), a 32 kHz crystal (Y458), and a battery (BT275). Refer to the *Calendar (Real Time Clock)* circuit description in Section 4 for a detailed description of circuit operation.

Clock Tests

The following tests check the clock circuitry and associated data and address buses.

- **Clock Register Test**--Tests that clock read/write registers can be accessed; tests for bad data lines.
- **Clock Timing Test**--Tests the basic operation of the hundredths register and the oscillator circuit.
- **Clock Functional Test**--Tests that the Signetics® calendar chip is operational.

NOTE

The clock calendar circuits lose six seconds for each minute that they are exercised. Thus, if you run these tests , i.e., loop on test(s) for an extended period, check and reset the date/time using the procedure described in Section 5.

Routine 0: **CLOCK REGISTER TEST**

Description: Reads and writes test patterns 00, AA, and FF to (1)check that the calendar chip read/write registers can be accessed, and to (2)check for bad data lines.

Algorithm:

1. Save current value of the clock registers.
2. Write first pattern to all read/write registers (mask off unused bits).
3. Test each register for correct data (mask off unused bits).
4. If pass, write in the next pattern.
5. Go to next register and repeat steps 3-4 until last pattern is tested.
6. Restore registers to original value.

Path Tested: U350 (the calendar IC), data lines IOD[00:07], address lines GBA[1:2] and BBA[1:5], read enable line (CALENDARR), and write enable line (CALENDARW).

Index 1: Data has been written to the register and is now being read back.

Problem: The value read back was not what was written.

Actual: The value read from the register.
Expected: The value written to the register.
Address: Address of the clock register that is being tested.

Action: If value read back = FF, then check the read write lines (CALENDARR and CALENDARW).

If Actual = 55 and Expected = AA, check the following:

- address lines (BBA[1:5].
- check data lines associated with the failing bits.
- replace U350 (the calendar chip).

Routine 1: **CLOCK TIMING TEST**

Description: Sets the clock calendar hundredths register to zero, starts calendar for one tenth of a second, then stops calendar. The contents of the hundredths register is then checked to be equal to 10 (one tenth of a second).

Algorithm:

1. Set hundredths register to zero (0).
2. Start calendar for 1/10 of a second (as timed by an assembly level routine), then stop the calendar.
3. Read contents of hundredths register and check if = 10.
4. Start the calendar.

Path Tested: Checks all calendar chip circuitry, except for the battery.

Index 1: The hundredths register was set to zero (844801 = 0).

Problem: Contents of the hundredths register did not equal 0.

Actual: The value read from the hundredths register.
Expected: 0 (zero)
Address: the address of the hundredths register.

Action: If the clock register test (Routine 0) passes, then replace U350 (ICM7170).

Index 2: The calendar was started and timed for 1/10 second, then stopped. The hundredths register is then read and checked for a value of 10.

Problem: The hundredths register did not = 10 (1/10 sec.).

Actual: The value read from the hundredths register.
Expected: 10 (1/10 sec.)
Address: The address of the hundredths register.

Action: If the expected value does not = FF or 00, check the following:

A. Put this routine into a loop and adjust C455 in small increments (cw and/or ccw) until test passes. Capacitor C455 is adjustable only on the MPU board with 2 Mbyte RAM. If test now runs, go to Step B; if test still will not run, go to Step C.

B. If test passes after performing Step A, run the *Clock Adjust Routine* for an accurate adjustment (refer to adjustment description in Section 5 for procedures). Or, turn C455 one direction until the Clock Time Test fails. Note the position of C455. Now, turn C455 in the other direction until the test fails once again, Note this position of C455, then set C455 in the middle of the two points of failure.

C. If the Clock Time test still will not pass, use scope to check for a 32 kHz signal on pins 10 and 9 of U350 (ICM7170). If frequency equals 32 kHz, adjust C455 noting change in frequency. If no change in frequency, replace C455.

If no change after replacing C455, replace U350.

Action: If the expected value = FF or 00 and if the Clock Register Test (Routine 0) passes, then replace U350 (ICM7170).

Routine 2: **CLOCK FUNCTIONAL TEST**

Description: Sets up time for maximum count. Hundredths = 99, seconds = 59, date = 31, etc. After set-up, the routine starts the clock for 1/100 second and checks that the times all rolled to their minimum value.

Algorithm:

1. Save present time.
2. Load maximum values into all the time registers:

Hundredths	= 99	
Seconds	= 59	
Minutes	= 59	
Hours =	= 23	
Date	= 32	
Month	=	= 12
Year	= 99	
Weekday	= 7	

3. Start clock for 1/100 sec.
4. Read time registers for minimum values.
5. Restore original time.

Path Tested: U350 (ICM7170)

Index 1: Check hundredths register. Expected = 0.
Index 2: Check seconds register. Expected = 0.
Index 3: Check minutes register. Expected = 0.
Index 4: Check hours register. Expected = 0.
Index 5: Check date register. Expected = 1.
Index 6: Check months register. Expected = 1.
Index 7: Check year register. Expected = 0.
Index 8: Check weekday register. Expected = 1.

Problem: Register did not roll over after running for 1/100 sec.

Expected: See index information, this test.
Address: Address of the applicable register.

Action: If this test (Routine 2) fails, but Routines 0 and 1 pass, then replace U350 (ICM7170).

TEST AREA: RS232 TESTS

Circuit Overview

Refer to Schematic 11. RS232 circuitry on the MPU board consists of a Signetics® 2681 DUART, two MC1489s, and one MC1488. Host and keyboard interrupts are input directly to the interrupt multiplexer circuitry. Refer to *Keyboard and Host Interface* description in Section 4 for a detailed description of RS232 circuit operation.

Test Description

The RS232 tests consist of four routines that test the keyboard and host RS-232C ports. These routines are:

- UART Existence test
- Internal UART Loopback test (for console port)
- Internal UART Loopback test (for host port)
- External Loopback test (for host port)

Routine 0: **HOST CHANNEL EXISTENCE TEST**

Description: Verifies that the host channel (channel B) exists and can be accessed.

Algorithm:

1. Select mode register 1 (write 10H to the command register, address 844015H).
2. Write in data pattern.
3. Select mode register 2 (automatically selected after mode register 1 is accessed).
4. Write in complimentary data pattern.
5. Test mode register 1 for correct data (read from 844011).
6. Test mode register 2 for correct data (read from 844011).
7. Restore UART hardware.

Path Tested: Verifies IOD[0:7] data lines to DUART chip; verifies CSN, RDN, and WRN signal lines.

Index 1: The data that was previously written to mode register 1 is read back from mode register 1 (address 844011).

Problem: If actual = 00 or FF, then channel B of the DUART cannot be accessed.

Action: Check for the following signals at the DUART: RDN(L), pin 9, WRN(L), pin 8, CSN(L), pin 35. If these signals appear OK, replace 2681 DUART.

Problem: If actual = XX (undefined), then find the bits in actual that are different from the expected. (The data bits correspond to the IOD[0:7] inputs to the DUART.)

Example: If actual = EA and the expected = AA, then IOD6 (bit 6) is bad.

Action: Check failing IOD data line (see above example), or replace 2681 DUART.

Index 2: The compliment data that was previously written to mode register 2 is read back from mode register 2 (address 844011).

Problem/Action: See ***Index 1*** **Problem** and **Action**.

Routine 1: **CONSOLE (KEYBOARD) PORT INTERNAL LOOPBACK TEST**

Description: This routine sets the DUART to local mode and a character string is internally transmitted in channel A (the keyboard channel).

Algorithm:

1. Set a pointer to channel A.
2. Reset the UART.
3. Disable the UART interrupts.
4. Put UART in internal loopback mode.
5. Set baud to 9600
6. Test that the status register is cleared.
7. Enable transmitter.
8. Test status register for transmitter ready and empty.
9. If transmitter ready, send a character until end of string.
10. If receiver ready, read a character until end of string or until time-out condition.
11. Test if received string is same size as transmitted string.
12. Test received string for correct data.

Path Tested: Tests channel A internal operation of the DUART. This routine requires that the DUART can be addressed and programmed (by the Microprocessor), as verified by *Routine 0*, previously described.

Index 1: The error bits of the status register are cleared and the transmitter and receiver are disabled via commands to the DUART command register. The status register is then checked for the following;

- no errors
- receiver and transmitter is not ready
- FFULL is cleared
- transmitter is empty.

Problem: The actual data is the returned value of the status register. Any bit set (bit = 1) in the status register indicates an internal DUART problem. Refer to Table 9-2.

Table 9-2
Status Register
(Channel A, Keyboard, Address = 844003)
(Channel B, Host, Address = 844013)

BIT 7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
received break	framing error	parity error	overrun error	TxEMT	RxRDY	FFUL	RxRDY

0 = not set
1 = set

Action: Replace the 2681 DUART.

Index 2: The UART transmitter is enabled and the status register is checked for TxEMT (bit 3) and TxRDY (bit 2) = OCH.

Problem: Actual does not = OCH. This indicates a DUART internal problem.

Action: Replace 2681 DUART.

Index 3: The test string was transmitted and the received string was checked for the correct length.

Problem: Received (actual) data string does not equal transmitted (expected) data string. Any errors in actual data string indicates a problem internal to the DUART.

Action: Replace the 2681 DUART.

Index 4: Data transmission was completed and the correct number of characters were received. The character string is now checked for the correct data.

Problem: Received (actual) data does not equal transmitted (expected) data. Any errors in actual data indicates a problem internal to the DUART.

Action: Replace the 2681 DUART.

Routine 2: **HOST PORT INTERNAL LOOPBACK TEST**

Description: This routine sets the DUART to local mode and a character string is internally transmitted in channel B (the host channel).

Algorithm:

1. Set a pointer to channel b.
2. Reset the UART.
3. Disable the UART interrupts.
4. Put UART in internal loopback mode.
5. Set baud to 9600
6. Test that the status register is cleared.
7. Enable transmitter.
8. Test status register for transmitter ready and empty.
9. If transmitter ready, send a character until end of string.
10. If receiver ready, read a character until end of string or until time-out condition.
11. Test if received string is same size as transmitted string.
12. Test received string for correct data.

Path Tested: Tests channel B internal operation of the DUART. This routine requires that the DUART can be addressed and programmed (by the microprocessor), as verified by *Routine 0*, previously described.

Index Information: Refer to *Index 1-4* for Routine 1.

Routine 3: **HOST EXTERNAL LOOPBACK TEST**

Description: Performs an external loopback test on the host port. This routine requires that you connect an external loopback connector to the host connector, J945, on the back panel before you start the test. (The loopback connector has pin 2 (TRANDATA) connected to pin 3 (RECDATA) and pin 5 (CTS) connected to pin 20 (DTR).

Algorithm:

1. Set a pointer to the ports get_char( ) and put_char( ) routines.
2. Initialize the transmit character string.
3. Send a character.
4. Test to see if the DUART received the character.
5. If no character received, check status word and set the index accordingly.
6. If a character was received, read and save the character.
7. Repeat steps 3-6 until end of string or timed out.
8. Test that the received string equals the transmitted string.

Path Tested: Tests the data transmit and receive lines from the DUART, to the loopback connector and back to the DUART. Signal lines tested are TRANDATA, RECDATA, RTS, and DTR. Also tested are the interrupt signals IRQ, RECINT, and TRANINT.

Index 1: A character is transmitted and the receiver is checked to see if it received the character. If no character is received before a time-out, the test fails.

Problem: The DUART channel B never received a character.

Action: Run the Host Internal Loopback Test (Routine 0). If it passes, check the RECDATA/TRANDATA path (from pin 11 of the DUART to pin 2 of the loopback connector, through pin 3 of the loopback connector to pin 10 of the DUART.)

Index 2-6: The DUART detected an error after a character was received. The DUART status register is examined and the test index number is set accordingly.

Index 2: Actual = 010H

Problem: Overrun error caused by a receiver buffer overflow.

Index 3: Actual = 20H

Problem: Parity error. A character was received with in incorrect parity bit.

Index 4: Actual = 40H

Problem: Framing error. No stop bit received.

Index 5: Actual = 80H

Problem: Received break. An all-zero character was received without a stop bit.

Index 6: Actual is any combination of the above.

Problem: For example, if actual = 30H then there is a combined overrun and parity error.

Action: For any of the above problems, check the RECDATA/TRANDATA signal path from the DUART through the loopback connector, back to the DUART.

Index 7 Transmission of the data string is complete and the received string is compared to the transmitted string.

Problem: Actual (received string) does not equal expected (transmitted string).

Action: Check the RECDATA/TRANDATA signal path from the DUART through the loopback connector, back to the DUART.

TEST AREA: GLUE

Circuit Overview

The GLUE gate array, U518, supports the 68010 processor as it interacts with the analyzer system. It does the following:

- Provides processor support circuitry such as address decoding and interrupt vector generation, bus error (BERR detection and memory management), and system clocking.
- Provides DRAM control
- Provides address decoding for the hard disk controller interface.
- Provides some COMM pack support logic.
- Provides audio tone generator.
- Provides DMA control between DRAM and the system disk.

The specifics of GLUE gate array operation are described throughout the circuit descriptions provided in Section 4.

Test Descriptions

The GLUE Area consists of the following tests:

- GLUE Register Test
- GLUE Interrupt Test
- GLUE Beeper Test

Routine 0: **GLUE REGISTER TEST**

Description: Test patterns are written into the GLUE gate array's read/write registers, and then read back.

Algorithm:

1. Save current value of the GLUE registers.
2. Write first pattern to all read/write registers (mask off unused bits).
3. Test each register for correct data (mask off unused bits).
4. If pass, write the next pattern in.
5. Go to next register and repeat Steps 3-5 until last pattern is tested.
6. Restore the registers to their original value.

NOTE: The test patterns are: FFFF, 5555, AAAA, 0000.

Path Tested: Tests the basic interconnect signals and circuits between the GLUE gate array and the 68010 processor (KA[1:22], KD[00:15], KAS/, KUDS/, KLDS/, KRW, and DTACK/).

Index 1: Data has been written to the GLUE read/write register and is now being read back to the Microprocessor.

Problem: The value read back was not what was written.

Actual: The value read from the register.
Expected: The value written to the register.
Address: Address of the register being tested.

Action: Perform the following as indicated:

- If value read back = FFFF, then check the KRW signal line.
- If actual = AAAA and expected = 5555, then check the address lines KA[1-5].
- Check the data lines associated with the failing bits.
- Replace U518 (GLUE gate array).

Routine 1: **GLUE INTERRUPT**

Description: This routine sets individual kernel interrupts and then tests them from their source via the GLUE's interrupt status register. Table 9-3 lists the interrupt signals tested in the order in which they are tested. Refer to MPU Schematic 8 and the MPU Detailed Block Diagram to trace interrupt signal paths.

Table 9-3
Interrupts Tested

Interrupt	Signal Name
Console knob tick	CLK_TICK
Keyboard Receive	KBRECINT
RS232 Receive	RECINT
Keyboard Transmit	KBTRANINT
RS232 Transmit	TRANINT
DUART IRQ	IRQ
Floppy IRQ	FLOPPY IRQ
Comm Pack	PAKINT
Hard Disk	HARDDISKIN~
Video Gate Array	VIDEO_INT
TekLink Gate Array	COMINT

The following interrupt signals are not tested:

- PFINT (Power Fail Interrupt)
- FLOPPY_DRQ
- KILL_POWER
- LOWBAT (Low Battery)
- DEBUG_INT (Debug NMI)

Algorithm:

1. Save the current value of the GLUE interrupt mask register (0x85F17E).
2. Mask off interrupts to the 68010 except NMI and POWER FAIL (0x85F17C).
3. Run individual interrupt routines.

4. Run DUART-generated interrupt tests.
    a. Turn off all interrupt bits in DUART OPR.
    b. Read interrupt status register.
    c. Check that no interrupts are asserted.
    d. If no interrupts, then continue.
    e. Assert CLOCK_TICK_INT bit.
    f. Read interrupt status register.
    g. If interrupt present then continue, else report error.
    h. Clear output port.
    i. Repeat Steps e through h for the following interrupts: Keyboard_REC_INT, RS232_REC_INT, KEYBOARD _XMIT_INT, and RS232_XMIT_INT.
    j. Set IMR to assert INTRN on TXRDYB empty.
    k. Read interrupt status register.
    l. If interrupt present, then continue; else report error.
5. Run Floppy IRQ interrupt test.
    a. Write force_int command to floppy command port.
    b. Wait 100 microseconds for command delay.
    c. Readback interrupt status register.
    d. If interrupt present, then continue; else report error.
    e. Write clear_cmd to floppy controller/formatter.
    f. Read floppy status register to clear interrupt.
6. Run COMM Pack interrupt test.
    a. Save old value of floppy select latch (write only register).
    b. Write value to floppy select latch (which will generate interrupt if no Comm Pack is installed).
    c. Check if Comm Pack is installed and reset PK/ if true.
    d. Readback interrupt status register.
    e. If interrupt present, then continue; else report error.
    f. Restore original value of floppy select latch.
7. Run Hard Disk Interrupt test.
    a. Check if hard disk is installed.
    b. If installed, then test for interrupt.
    c. Send a Seek-to-Current command to disk.
    d. Wait for either interrupt to occur or to time-out.
    e. Readback interrupt status register.
    f. If interrupt present, then continue; else report error.
    g. Read hard disk status register to clear interrupt.

8. Run Video Gate Array Interrupt test.
    a. Set the video array interrupt register to generate an interrupt on each vertical sync pulse.
    b. Wait long enough to ensure a sync pulse.
    c. Read back interrupt status register.
    d. If interrupt present, then continue, else report error.
    e. Disable video interrupts and clear window interrupts.
    f. Re-enable Video array interrupts.
9. Run TekLink Gate Array Interrupt test.
    a. Clear any modules assigned for buffer transfers.
    b. Wait until command is completed.
    c. Put TekLink gate array in its diagnostic mode.
    d. Set diagnostic hardware for immediate write.
    e. Write a module number.
    f. Wait until command is completed.
    g. Set interrupt bit to start internal transfer.
    h. Wait until interrupt or time-out out occurs.
    i. Readback interrupt status register.
    j. If interrupt present, then continue; else report error.
    k. Read immediate data register to clear interrupt.
    l. Turn off array's diagnostic mode.
10. Report pass status to test controller if all routines pass.
11. Reset IMR and clear port bits in DUART.
12. Restore DUART to original state.
13. Restore original interrupt mask value

Path Tested: This routine tests the following:

- GLUE array's Interrupt status and mask registers,
- interrupt paths through the GLUE gate array,
- interrupt multiplexer (MPU Board Schematic, Sheet 8) and associated interrupt circuits on the MPU board.

Index 1: The output port on the DUART has been cleared. Checking that no interrupts are present.

Problem: Status register readback as non-zero.

Actual = the value read back from GLUE gate array Interrupt status register.
Expected = zero
Address = the interrupt status register being tested (0x85F17E).

Action: If status register read back as non-zero, check the following:

- If any of data bits 0, 1, 4, 6, 7, or 11 are true, check the corresponding output of the DUART chip.
- If any other data bit is true (excluding bits 14 and 15), check interrupt source (not all interrupts are DUART-related).

Index 2: **Problem:** The Clock_Tick interrupt did not occur.

Actual = the value read back from GLUE gate array interrupt status register.
Expected = 0x0800
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on the test.
2. Check for toggle on the CLK_TICK output of the DUART (pin 13).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U360, pin 12).
4. If CLK_TICK signal is at pin 1 of DUART, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array. (Check that the INTH and INTL signals from the interrupt multiplexer delay lines are fed into the GLUE gate array.) The interrupt output from a multiplexer chip is selected as shown in Table 9-4.

Table 9-4
Selecting Interrupt Multiplexer Output

PTR3	PTR2	PTR1	Output
L	L	L	D0/
L	L	H	D1/
L	H	L	D2/
L	H	H	D3/
H	L	L	D4/
H	L	H	D5/
H	H	L	D6/
H	H	H	D7/

Suspect delay lines DL355 or DL560, interrupt multiplexers U360 or U555, or GLUE gate array U518.

5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, do the following:

   a. Read the actual to determine the unwanted interrupt.
   b. Loop on the test (GLUE Interrupt Test) and, using scope or logic analyzer, see if the unwanted interrupt is either stuck "high" or is occurring at the same time as the unwanted interrupt.
   c. If either condition in Step b is occurring, trace the unwanted interrupt back to its source.
   d. If the unwanted interrupt signal appears OK at the input to the interrupt multiplexer, replace the GLUE gate array.

Index 3:

Problem: The Keyboard_Receive interrupt did not occur.

Actual = the value read back from the GLUE arrays interrupt status register.
Expected = 0x0002
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the KBRECINT output of the DUART (pin 27).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 2).
4. If KBRECINT at pin 27 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 4:

Problem: the RS232_Receive interrupt did not occur.

Actual = the value read back from the GLUE array's interrupt status register.
Expected = 0x0080
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the RECINT output of the DUART (pin 14).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 1).
4. If RECINT at pin 14 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 5:

Problem: The Keyboard_Transmit interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt Status register.
Expected = 0x0001
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the KBTRANINT output of the DUART (pin 26).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 2)
4. If KBRECINT at pin 26 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 6:

Problem: The RS232_Transmit interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.

Expected = 0x0040

Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the TRANINT output of the DUART (pin 15).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 3).
4. If KBRECINT at pin 15 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 7:

Problem: The IRQ interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0010
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following

1. Loop on test.
2. Check for toggle on the IRQ output of the GLUE gate array.
3. If no toggle, replace the GLUE gate array, else follow toggle to the interrupt multiplexer (U555, pin 13).
4. If IRQ OK from GLUE gate array, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 8:

Problem: The Floppy_IRQ interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0400
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on FLOPPY_IRQ between pin 28 of floppy controller and pin 14 of U360..
3. If no toggle, replace the floppy controller integrated circuit.
4. If FLOPPY_IRQ at U360, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 9:

Problem: The COMM pack interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0020
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of PAKINT from U370 pin 11 to U555 pin 15.
3. If no toggle, trace PAKINT from U370 back to COMM pack.
4. If PAKINT at U555, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index A:

Problem: The Hard_Disk interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0008
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for HARDDISKINT from J120 pin 5 to U555 pin 12.
3. If no toggle at J120 pin 5, troubleshoot Hard Disk Controller board. (Refer to Hard Disk Module diagnostic tests later in this section.)
4. If HARDDISKINT at U555 pin 12, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index B:

Problem: The Video interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0100
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of VIDEO_INT from pin 35 of Video gate array to U360 pin 2.
3. If no toggle, replace the Video gate array.
4. If VIDEO_INT at U360, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index C:

Problem: The TekLink interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0200
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of COMINT from TekLink gate array pin 21 to U360 pin 4.
3. If no toggle, replace the TekLink gate array.
4. If COMINT at U360 pin 21, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Routine 2: **BEEPER**

Description: This routine causes the beeper circuit to "beep."

Algorithm: 1. Exercise the beeper circuit with a 2 kHz signal lasting 0.7 seconds.

Path Tested: Tests beeper circuitry in the GLUE gate array and discrete circuitry on the MPU Board. Specific component tests are U518 (GLUE gate array), Q285, YG190, R296, R295, and C290.

Index 1 The"beeper on" bit in the beeper register (in GLUE gate array) did not get set.

Actual: = Beeper on bit "12" not set.
Expected: = Bit 12 set.
Address: = Beeper register.

Action: Replace GLUE gate array.

Index 2 The "beeper on" bit in the beeper register (in GLUE gate array) did not get reset.

Actual: = Bit 12 high.
Expected: = Bit 12 low.
Address: = Beeper register.

Action: Replace GLUE gate array.

TEST AREA: FLOPPY

Circuit Overview

The floppy interface circuitry consists primarily of a Western Digital® 1770 Floppy Controller/Formatter and associated circuits. This circuitry is shown on MPU Board Schematic Sheet 10. Refer to the *Floppy Interface* description in Section 4 for a detailed explanation of circuit operation.

Test Descriptions

The floppy disk interface circuitry is verified by the following tests:

- Controller Existence test
- Ready test
- Motor test
- Track 0 test
- Read test

The Manual Floppy Test Area contains three additional floppy tests. Refer to Manual Floppy Test Area later in this section for test descriptions.

DISK ERROR CODES

The following errors appear as actual data for failed disk commands. Not all failed tests use these codes. Refer to the *Index* information for specific failed test information.

0001 **Disk Busy.** The floppy controller is currently executing a command.

0004 **Track 00.** (Restore and Step Commands) The drive's head is at track 0.

0004 **Lost Data.** (Read and Write Commands) During a read command, this error code means that data was not read from the controller's data register to the BD[00:15] data bus before the controller read additional data from the disk.

During a write command, this error code means that data was not written to the controller's data register in sufficient time for the controller to write the data to the disk.

0008 **CRC Error.** All the disk diagnostic commands use the verify flag. This causes the controller to check the CRC (cycle redundancy check) of the track. It then sets this error if the CRC is bad. A CRC Error can be caused by any one of the following:

- bad disk
- bad read head
- CRC circuitry in the controller/formatter is bad

0010 **Record not Found.** All the disk diagnostic commands use the verify flag. The verify flag causes the controller/formatter to compare the head location (track and sector number of the head location), against the head location in the track and sector register. If they do not match, the Record not Found error is set. A Record not Found error can be caused by any one of the following:

- an unformatted disk
- disk read/write head cannot be stepped
- wrong side of disk is selected (odd tracks = side 1; even tracks = side 0)
- bad read head
- bad WD1772 controller/formatter

0040 **Write Protect.** A write command was given to a write-protected disk. If disk is not write-protected, and this error still occurs, check the WPROTECT (Write Protect) signal line at J170, pin 20.

0080 **Motor On.** This occurs when the floppy drive motor reaches operating rpm.

0100 **No FLOPPY_IRQ.** This code occurs whenever the FLOPPY_IRQ signal (pin 28 of controller/formatter) fails to occur at the completion of a disk command.

0200 **No FLOPPY_DRQ.** This code occurs whenever the FLOPPY_DRQ signal (pin 27 of controller/formatter) fails to occur. FLOPPY_DRQ should occur each time the controller/formatter wants the MPU's microprocessor to read/write data either to or from the data registers (during read or write commands).

0300 **No Disk Installed.** If this error occurs with a disk installed, run the Disk Change test under *Manual Floppy Area.*

GENERAL TROUBLESHOOTING INFORMATION

If a disk error code occurs, consider the following general troubleshooting guidelines before exercising the floppy diagnostic tests.

1. Ensure a good (formatted) disk is installed.
2. Check that the proper drive has been selected.

   J170 pin 10 = drive select 0
   J170 pin 12 = drive select 1

3. Check the signal paths of the failed test for valid levels (see index information of failed test for details).

Routine 0: **FLOPPY CONTROLLER EXISTENCE TEST**

Description: Checks that the controller/formatter can be accessed; verifies the eight data lines IOD[00:07] that connect to the controller/formatter.

Algorithm:

1. Read track register and save value.
2. Write pattern in the track register.
3. Write complimentary pattern in the sector register.
4. Read track register and test for correct data.
5. Read sector register and test for correct data.
6. Restore track register with original data.

Path Tested: Tests data lines IOD[00:07], address lines GBA[1:2], and control signals LBRW and 1772_SEL.

Index 1: Read back data from the track register (address 845f03). Actual = read data.

Problem: Actual data does not = expected data.

Action: If actual does not = expected,

- Check that IOD[00:07], 1772_SEL, and GBA[1:2] are functioning at their inputs to the controller/formatter.
- Replace the WD1772 controller/formatter.

Routine 1: **FLOPPY READY TEST**

Description: Tests that the floppy drive spins up and is ready for read/write operations.

Algorithm:

1. Issue Restore command.
2. Wait for disk to become ready (address 844C01 bit 1).
3. Wait for disk to become not ready.

Path Tested: Tests the READY signal line from the disk drive to J170 pin 34, through the floppy disk latch to the IOD[1] data line.

Index 1: A Restore command was given causing the disk to spin up and become ready.

Problem: The Restore command returned an error (actual data = disk error code).

Action: Refer to the *Disk Error Codes* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 2: Wait for disk to become ready after a command was given.

Problem: Disk does not become ready before the test times out. Address 844c01 bit 1 is high (bit 1 low = ready). The ready bit should go low (ready) after the disk has reached operating speed.

Action: Check READY signal line from the floppy drive (J170, pin 34) to floppy disk control latch, pins 6 and 14.

Index 3: **Problem:** Disk did not go "not ready" before the test times out. Address 844c01 bit 1 = low. The READY bit should go high after the command has finished and the motor has stopped spinning.

Action: Check the READY signal line from the floppy drive (J170, pin 34) to floppy disk control latch, pins 6 and 14.

Routine 2: **FLOPPY MOTOR TEST**

Description: Tests the MOTOR ON/ signal line from the controller/formatter. This line goes high when the driver motor is to be turned on; low when it is off.

Algorithm:

1. Give Restore command with MOTOR ON flag set.
2. Check the controller's status register to ensure that the motor on bit gets set before the test times out (motor is on).
3. Wait for disk not ready with time-out (command is completed).
4. Check that the controller's status register motor on bit gets reset before the test times out (motor is off).

Path Tested: The MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16 to the floppy drive unit.

Index 1: The Restore command was given to the floppy drive.

Problem: The Restore command returned an error. The actual data = disk error code.

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 2: Check the controller's status register to ensure that the motor on bit gets set before the test times out (motor is on).

Problem: Motor on (controller status register bit 7) does not go high.

Action: Check the MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16, to the floppy drive unit.

Index 3: Wait for the disk drive to become ready.

Problem: the disk did not become ready.

Action. Run the Floppy Ready test (Routine 1).

Index 4: Check that the controller's status register Motor on bit gets reset before the test times out (motor is off).

Problem: Motor is on (controller's status register bit 7 never goes low).

Action: Check the MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16 to the floppy drive unit.

Routine 3: **FLOPPY TRACK 0 TEST**

Description: Tests that the TR_0 (Track 0) signal line from the floppy drive goes low when the head is positioned at Track 0.

Algorithm:

1. Initiate Restore command.
2. Check that the controller's status register track 00 bit is set.
3. Step head to track 1.
4. Check that the controller's status register track 00 bit is low.

Path Tested: The TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

The STEP/ signal pin 16 of the controller/formatter, to J170, pin 20.

Index 1: The Restore command was given to the disk drive. This causes the heads to move to Track 0.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 2: Check that the controller's status register track 0 bit (bit 2) is set.

Problem: Controller's status register shows track 0 Bit 2) is not set.

Action: Check the TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

Index 3:

Use the Seek command to move the disk drive's read/write head to Track 1. This causes the TR_0 signal line to go high and the controller's status register track bit (bit 2) to go low.

Problem: The Seek command returned an error. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 4:

Check that the controller's status register Track 0 bit (bit 2) is set low.

Problem: The controller's status register shows that bit 2 remains high.

Action: Check the TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

Routine 4: **FLOPPY READ TEST**

Description: Checks that a simple disk read can be performed on side 0 with no errors.

Algorithm:

1. Allocate memory for the read buffer.
2. Initiate Restore command.
3. Read track 0, sector 1.

Path Tested: The RDATA (Read Data) signal from J170, pin 30, through the floppy disk control latch, to pin 19 of the controller/formatter.

The WGATE (Write Gate) signal from pin 21 of the controller/formatter to J170, pin 24.

Index 1: The system call "allocMem( )" is used to allocate one sector's worth of RAM for the disk read test.

Problem: The system call "allocMem( )" failed. (The actual data = the operating system error code.) Failure could be caused by one of the following:

- the system has insufficient memory
- a program is overwriting either the stack or its own RAM boundaries.

Action: Reboot the system and rerun the test.

Index 2: A Restore command was given to insure that the read/write head and track register are correct.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 3: Read Track 0, Sector 1 (side 0).

NOTE

Data read from the disk is not important. However, it must be read without error.

Problem: The Read command returned an error. (the actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

TEST AREA: TEK COMM (TEKLINK INTERFACE)

Circuit Overview

TekLink is a high-speed serial data interface used between the MPU board and acquisition modules. TekLink circuitry is shown on MPU board schematic sheets 15-19. The primary electrical component is the TekLink gate array. Other circuits consist of: TekLink RAM, clock, SIGNAL[1-4] line buffers, SYS-TRIG and level shift, and TRIG and RUN delay.

Test Description

The TekLink gate array and associated circuitry is exercised using the following diagnostic tests:

- Register test
- Immediate Read test
- Interrupt test
- RAM test
- Buffer Transfer tests
- Tek Event (SIGNAL[1:4]) tests

Routine 0: **REGISTER TEST**

Description: Writes four patterns into TekLink gate array registers.

Algorithm:

1. Turn on the gate array's diagnostic mode and set the write test bit in the diagnostic register, F04014 = 21H.
2. Write the first data pattern to all the OPCOMM registers. (Leave diagnostic mode and write test selected in the diagnostic register.
3. Loop through reading the registers. Skip the following:
   - read only registers
   - immediate busy flag
   - interrupt address
4. If the previous data was correct, write in a new pattern.
5. Repeat the above for all four data patterns (0xFFFF, 0x5555, 0xAAAA, and 0x0000).

Path Tested: Tests the TekLink gate array registers, BBA[1:14] address lines, BD[00:15] data lines, BRW read/write signal, and BLDS/ data strobe.

Index 1: The last data written to the register is read back, and if it passes, the next pattern is written to the register.

Problem: Actual does not equal expected.

Actual: Value read back from the register does not equal expected.
Expected: The value that was written to the register.
Address: The address of the register.

Action: If actual does not equal expected:

- check the data lines, BD[00:15], associated with the failed bit(s).
- if FFFF is the actual data, check the read/write line BBRW (it could be bad).
- If an inappropriate data pattern other than FFFF is read back, one or more of the address lines could be bad. Specifically check BBA[1:5]. For example: actual = 5555 and expected = FFFF at address F04002.

Routine 1: **IMMEDIATE READ TEST**

Description: This is an internal test of the TekLink gate array that uses the array's internal diagnostic mode. When initiated, the internal diagnostic mode tri-states outputs and loops the out-going data back as in-coming data.

This test initiates four immediate read commands using a different test pattern for each (0xFFFF, 0xAAAA, 0xB555, and 0x8000). The array's diagnostic circuitry loops the out-going address back as incoming data. The incoming data is then read in the immediate data register. The process is repeated for each internal and external application module connected to the MPU board.

Algorithm:

1. Select TekLink diagnostic mode (f04014 bit 0 =1).
2. Write first pattern into the immediate address register.
3. Select first acquisition module.
4. Wait for command to finish (check immediate busy flag at f0400a).
5. Test that the address from the immediate address register appears in the immediate data register (f04006).
6. Repeat transfer until all four address patterns are transferred.
7. Repeat the four address pattern transfers for all the application modules (0-7 internal, and 0-7 external).
8. Turn off the array's diagnostic mode.

Path Tested: The internal TekLink gate array circuits.

Index 1: The immediate busy flag is checked to ensure there is no immediate command in progress. If an immediate command is in progress, the routine waits (with time-out) until function of the current immediate command is completed.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

NOTE

Test times out without resetting the immediate busy flag.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 2: The test address was loaded into the immediate address register and the module number loaded into the immediate module register. This causes the immediate read to be executed and the immediate busy flag to set. This index checks that the immediate busy flag is set.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 3: Test that the immediate command finishes by waiting (with time out) until the immediate busy flag is reset.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 4: With the immediate read completed, check that the immediate address was looped back to the immediate data register.

Problem: The address was not read into the immediate address register.

Actual = the data read back from the immediate data register.
Expected = the address that was written into the immediate address register.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Routine 2: **INTERRUPT TEST**

Description: Test the immediate write and acquisition module interrupt functions of the TekLink gate array. (Both write and interrupt functions are tested together because the TekLink diagnostic circuitry needs an immediate write to generate a module interrupt.)

Algorithm:

1. Select TekLink array's internal diagnostic mode (f04014 bit 0 =1).

2. With array's internal diagnostics on, initiate an immediate write. This loads the immediate data into the diagnostic shift register; the module grant is loaded into the diagnostics HS Shift register (the module grant is used later as a module interrupt).

3. On the next frame, the diagnostic shift register shifts out the immediate data (stored earlier as imm_data) into the immediate data shift register.

4. The routine waits for the CPU interrupt (end of module interrupt), after which it tests the interrupt address register as follows:

    a. checks for the correct module address received (same as the acquisition module selected for an immediate write).

    b. checks that the interrupt bit is set.

    c. Checks whether the acquisition module was an internal or external module (also selected during the immediate write).

5. Test that the interrupt data register contains the immediate write data (data was stored in the diagnostic register during the immediate write and was output as interrupt data during the interrupt).

6. Repeat above sequence for all connected internal and external modules, using a different data pattern for immediate data for each module tested. The first module tested is external Module 0; the last module tested is Internal Module 7. Acquisition modules are number as follows: External modules are numbered 0-7; internal modules are numbered 8-F. A module's number is determined by its physical location on the TekLink interface bus.)

Path Tested: Internal TekLink gate array interrupt circuits, the COMINT (Comm Interrupt) signal line, and interrupt circuits external to the TekLink gate array.

Index 1: The immediate busy flag is checked to ensure there is no immediate command in progress. If an immediate command is in progress, the routine waits (with time-out) until function of the current immediate command is completed.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register

NOTE: the routine times out without resetting the immediate busy flag.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 2: Test data was loaded into the immediate data register; an address (with bit 15 low, for immediate write), was loaded into the immediate address register; the location number of the acquisition module was loaded into the immediate module register. This causes the immediate read to be executed and the immediate busy flag to set. (This index checks that the immediate busy flag is set.)

Problem: The immediate busy flag was not set.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 3: Test that the immediate command finished by waiting (with time-out) until the immediate busy flag is reset.

Problem: The immediate busy flag was not set.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 4:

The interrupt bit in the array's diagnostic register is set causing the stored grant (from the previous immediate write) to be shifted out of the diagnostic handshake register on the HS line as an incoming, unsolicited grant (module interrupt). The Diagnostic Interrupt Service routine sets a flag that is checked by this test routine to verify that an interrupt was generated.

Problem: The interrupt flag was not set.

Actual = interrupt status flag
Expected = the flag is set to one
Address = the application module number

Action: Check the following:

1. If the address equals a module other than external 0, the interrupt circuits external to the TekLink gate array are working: the problem is inside the gate array.

2. If the address equals external 0, the problem is most likely interrupt circuits external to the gate array. To verify:

- Connect an oscilloscope to pin 21 of the TekLink gate array, put this routine into a loop, and check for a pulse at pin 21.
- If there is no pulse, replace the TekLink gate array.
- If there is a pulse at pin 21, go the the GLUE test area, select and run Routine 1, the GLUE interrupt test. Follow the diagnostic procedures for that test.

Index 5:

The Interrupt Service Routine reads the interrupt address register to determine which acquisition module caused the interrupt.

Problem: The interrupt address register did not contain the expected module number.

Actual = the value read from the interrupt address register.
Expected = the acquisition module number that was used earlier for the immediate write and that was loaded into the diagnostic handshake register. The acquisition module number is now used as the module interrupt when the interrupt bit was set in the diagnostic register. Also, bit 4 should be low, signifying that a module interrupt did not occur.
Address = the address of the interrupt address register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 6:

The Interrupt Service Routine reads the interrupt data register. This read action should clear both the interrupt signal line COMINT and bit 4 in the interrupt address register (module interrupt).

Problem: Bit 4 of the interrupt address register was not set (no module interrupt).

Actual = 0 (module interrupt)
Expected = 1 (no module interrupt)
Address = module number

Action: If Routine 0 (TekLink gate array Register Test) passes, replace the TekLink gate array.

Index 7:

The Interrupt Service Routine reads the interrupt data register. This register should contain the data that was originally placed in the immediate data register for the immediate write. (The array's diagnostic circuitry stored this data and routed it as module interrupt data.)

Problem: The interrupt data did not equal the data that was written to the immediate data register.

Actual = data read from the interrupt data register.
Expected = data written to the immediate data register.
Address = the number of module being tested.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Routine 3: **RAM TEST**

Description: This routine consists of three subtests:

- Data Bit Independence tests that no data lines are stuck, are open, or are shorted.
- Address Bit Independence tests that no address lines are stuck, are open, or are shorted.
- RAM cell tests that the TekLink RAM chips are functional.

Algorithm:

1. Data Bit Independence:

   a. A walking "ones" pattern is used for address bits ABR[0:15].

2. Address Bit Independence:

   a. FFFF is written to address 0.

   b. Write the address line number to the address where only that address line is asserted. for example:

   - Write 0 to address 1
   - Write 1 to address 2
   - Write 2 to address 4
   - Write 3 to address 8 . . . , and so on.

   c. After the last address is written to, return to 0 and check for correct data. If address 0 fails, the value read should correspond to the address line that is stuck either low or high.

   d. Test the remaining address lines. If the address fails, the value read back should correspond to the address line to which it is shorted.

3. RAM Cell Test.

   a. Six patterns are written to all memory locations and read back. The patterns are: FFFF, 5555, AAAA, CCCC, F0F0, and 0000.

Path Tested: Tests the following: the TekLink RAM from address f00000 to f04000 (two 8464 RAM chips; the addressing and data lines from the TekLink array (ABR[0:12] and R[0:15]); the addressing and data lines from the MPU's microprocessor to the TekLink array (BBA[1:14 and BD[0:15]).

NOTE

ABR[0] corresponds to BBA, ABR1 to BBA2, etc. Also, if there is a problem with the BBA address lines, the most likely problem is an open address line to the TekLink gate array.

Index 1: Data bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = F00000, the first address in Tek Comm memory.

Action: If data read back did not match the data written:

- If expected = a bit high and actual equals bit low, check to determine if the bit is shorted low.
- If expected = 0 and actual equals bit(s) high, check if the set bit(s) are shorted high or are open.
- If the failing bits appear to be OK, the problem could be in the RAM chip. Replace RAM CHIP U528 for bits 0-7, and U730 for bits 8-15.

Index 2: Address Bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = the address that corresponds to either one address line or no address lines active. Example:

- no address set = address 0
- address bit 0 set = address 1
- address bit 1 set = address 2
- address bit 2 set = address 4
- and so on. . .

Action: Analyze the following and troubleshoot accordingly:

- If address = F00000, expected = FFFF, and actual = a value of 1-12, then actual data indicates an address line that is stuck high or low, or is open. For example: If actual = 4, then either address line ABR[4] (TekLink buffer address) or BBA[5] CPU address) is bad.
- The actual and expected = the two address lines that are shorted to one another. Example:

  Address = F00008
  Actual = 3
  Expected = 2

  Then ABR[2] and ABR[3] are shorted to one another.

Routine 4: **BUFFER TRANSFER TESTS**

Description: Fills the array's A buffer with an incrementing pattern. The array is then set in diagnostic mode to transfer the A buffer contents to the B buffer, then back to the A buffer. After each buffer transfer is completed, an interrupt is generated and the buffer is tested for correct data.

Algorithm:

1. Initialize the A buffer RAM with pattern, and B buffer RAM to zeros.
2. Enable TekLink array's diagnostic mode.
3. Assign A buffer to an external module for download from B buffer (read).
4. Assign B buffer to an internal module for upload to A buffer (write).
5. Set A and B buffer pointer to start of memory (0x0000).
6. Perform two immediate reads (internal and external) to set up the array's diagnostic handshake register. (This is used by the array's diagnostic circuitry to generate interrupts.) Immediate data is ignored.
7. Set bit two (diag transfer) of the diagnostic register to one (1). This starts the buffer transfer.
8. Wait for the MPU's microprocessor to signal the end of the buffer transfer.
9. Test B buffer for correct data.
10. Repeat the above steps, only reversing the transfer from buffer A to buffer B, then repeat once again from buffer B to buffer A.

Path Tested: Tests the buffer transfer circuitry internal to the TekLink gate array.

Indexes 1-3: An immediate read is performed to internal module 0. Refer to the *Immediate Read Routine,* Routine 1, *Indexes 1-3.*

Indexes 4-6: An immediate read is performed to external module 0. Refer to the *Immediate Read Routine, Routine 1, Indexes 1-3.*

- Index 4, refer to Routine 1, Index 1
- Index 5, refer to Routine 1, Index 2
- Index 6, refer to Routine 1, Index 3

Index 7: The buffer transfer bit in the array's diagnostic register is set. This causes either the A buffer to transfer to the B buffer or the B buffer to transfer to the A buffer. When the transfer is complete, an interrupt (COMINT) is generated. The Interrupt Service Routine sets a flag signifying that the interrupt occurred.

Problem: The interrupt flag was not set.

Action: If the TekLink Interrupt Test (Routine 2) passed, replace the TekLink gate array; otherwise, follow the troubleshooting procedures described for the TekLink Interrupt Test.

Index 8: The A and B buffers are checked to ensure that data was transferred from one buffer to the other buffer.

Problem: The data read back from the destination buffer did not match data from the source buffer.

Actual = data read from the destination buffer.
Expected = data written to the source buffer.
Address = failing RAM address of the destination buffer.

Action: If the TekLink RAM Test (Routine 3) passed, replace the TekLink Gate Array.

Index 9: After the buffer transfer is completed, the buffer should not be assigned to any of the modules. Test the buffer assignment registers for bit 5 low (buffer not assigned). Note that the buffer assignment registers are read by the Interrupt Service Routine.

Problem: The A buffer assignment register bit 5 did not go low (buffer did not become "unassigned").

Actual = 1 (bit 5 of the buffer assignment register).
Expected = 0
Address = address of the A buffer assignment register.

Action: Replace the TekLink gate array.

Index A: Read description of *Index 9.*

Problem: Bit 5 of the B buffer assignment register did not go low (buffer did not become "unassigned").

Actual = 1 (bit 5 of the buffer assignment register).
Expected = 0
Address = address of the B buffer assignment register.

Action: Replace the TekLink gate Array.

Index B: Read the interrupt address register to check that the source of the interrupt was a buffer terminal count (all data transferred/received).

Problem: The interrupt address register did not have buffer A and buffer B terminal count bits set as the interrupt source.

Actual = bit 5 and/or bit 6 did not get set.
Expected = bit 5 and bit 6 set 60H.

Action: Replace the TekLink gate array.

Index C: Reading the interrupt address register should clear the source of the interrupt.

Problem: Bit 5 and/or bit 6 were not cleared when the interrupt address register was read.

Actual = Bit 5 and/or bit 6
Expected = 0

Action: Replace the TekLink gate array.

Routine 5 **Tek Event (SIGNAL[1:4] Test**

Description Each of the four SIGNAL lines is asserted independently and then read back to verify that only the asserted line is set.

Algorithm A logic one is walked across each SIGNAL line (Trig_100, VRS, VE1, VE2, VE3, and VE4).

F06000 = 3F = Trig_100 high, all other SIGNAL lines low
F06000 = 3C = VRS high, all other SIGNAL lines low
F06000 = 3A = VE1 high, all other SIGNAL lines low
F06000 = 36 = VE2 high, all other SIGNAL lines low
F06000 = 2E = VE1 high, all other SIGNAL lines low
F06000 = 1E = VE4 high, all other SIGNAL lines low
F06000 = 3e = All SIGNAL lines low

Path Tested ETRG from pin 18 of U720 to Trig_100 on pin 55 of U720
RUN_STOP from pin 19 of U720 to VRS on pin 100 of U720
EE1 from pin 64 of U720 to VE1 on pin 8 of U720
EE2 from pin 65 of U720 to VE2 on pin 34 of U720
EE3 from pin 20 of U720 to VE3 on pin 111 of U720
EE4 from pin 101 of U720 to VE4 on pin 93 of U720

Index 1 Asserted one of the SIGNAL lines.

Problem: A SIGNAL line did not get set or reset.

Actual = The state of the SIGNAL line.
Expected = The expected state of the SIGNAL lines.
Address = F06000; the SIGNAL bus register.

Action: First, determine which SIGNAL lines are set wrong by reading the actual and expected data. Then follow the SIGNAL line from its source (at U720) to where it is read back to U720. See *Path Tested.* You should be able to locate the problem somewhere between the signal source and its destination.

NOTE

All signals, except for ETRG, are inverted from the source to the readback at U720.

The actual and expected data correspond to the signals that are readback from Trig_100, VRS, VE1-VE4. For example:

1 = Trig_100
2 = VRS
4 = VE1
8 = VE2
10 = VE3
20 = VE4

Example: Actual = 0; Expected = 4. In this case, the VE1 SIGNAL line failed. The source of EE1 should be low and the destination of VE1 should be high.

TEST AREA: VIDEO GATE ARRAY

CIRCUIT OVERVIEW

Tests the operation of Video RAM and the Video gate array. (Video RAM is tested from address 86C000 to 87FFFF. Also tested are addressing and data from/to the Video gate array.)

NOTE

If the display is unreadable due to a display or video problem , you can display the results of the following tests by connecting an RS-232C terminal or printer to the RS-232C port. Set baud rate to 19.2 Kbaud.

Routine 0 **VIDEO RAM**

Description This routine consists of three subtests:

- Data Bit Independence tests that no data lines are stuck, are open, or are shorted.
- Address Bit Independence tests that no address lines are stuck, are open, or are shorted.
- RAM cell tests that the TekLink RAM chips are functional.

Video RAM is copied to system RAM before the test begins. It is copied back after the test is completed.

Algorithm

1. For Data Bit Independence, a walking "ones" pattern is used for address bits ABR[0:15].
2. For address Bit Independence, the following occurs:
   a. FFFF is written to address 0.
   b. Write the address line number to the address where only that address line is asserted. for example:
      - Write 0 to address 1
      - Write 1 to address 2
      - Write 2 to address 4
      - Write 3 to address 8 . . . , and so on.
   c. After the last address is written to, return to 0 and check for correct data. If address 0 fails, the value read should correspond to the address line that is stuck either low or high.

d. Test the remaining address lines. If the address fails, the value read back should correspond to the address line to which it is shorted.

3. For the RAM Cell Test, six patterns are written to all memory locations and read back. The patterns are: FFFF, 5555, AAAA, CCCC, F0F0, and 0000.

Path Tested

Tests the following: RAM chips U638 and U545 (graphics RAM), RAM chips U440 and U525 (character RAM), the Video gate array, video RAM address lines RA[0-14], microprocessor address lines BBA[1-16] (RA0 corresponds to BBA1, RA1 to BBA2, etc.) If this test indicates a problem with the BBA address lines, the most likely problem is an open line to the Video gate array.

Index 1

Memory is allocated for the video RAM copy.

Problem: System could not allocate memory.

Actual =82 = Insufficient memory
=83 = No free segments
=96 = System timed out waiting for free memory
Expected = 0
Address = N/A

Action: Use the RAM Operations menu to unload an application from RAM, then try the test again.

Index 2

Data Bit Independence test.

Problem:

Action: = the read back data
Expected: = the data written
Address:= 86C000, the first address in Video RAM

Action: If data read back did not match the data written:

- If expected = a bit high and actual equals bit low, check to determine if the bit is shorted low.
- If expected = 0 and actual equals bit(s) high, check if the set bit(s) are shorted high or are open.
- If the failing bits appear to be OK, the problem could be in a RAM chip. Replace RAM CHIP U525 for bits 0-7, and U440 for bits 8-15.

Index 3

Address Bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = the address that corresponds to either one address line or no address lines active. Example: no address set = address 86C000

Video RAM is accessed by WORDS only. The microprocessor address lines that correspond to the Video RAM address lines are offset by 1. For example: processor address 86C004 equals video RAM address of 1; processor address 86C008 equals video RAM address 2, etc.

Action: Analyze the following and troubleshoot accordingly:

- If address = 0, expected = FFFF, and actual = a value of 1-12, then actual data indicates an address line that is stuck high or low, or is open. For example: If actual = 4, then either address line RA[4] or BBA[5] is bad.
- If address = anything other than 0, then actual and expected = the two address lines that are shorted together. For example: If address = 86C008, actual = 3, expected = 2, then RA[2} is shorted to RA[3] or the processor addresss lines BBA3 and BBA4 could be shorted.

Index 4

RAM Cell Test

Problem: The data read back did not match the data written.

Actual: = the read back data
Expected = the data written
Address = the failing video RAM address

Action: Address and Data Bit Independence tests have passed so the problem is with one of the video RAM integrated circuits.

Routine 1 **VIDEO TEST**

Description This area consists of one test that "sets up" the Video gate array to test windowing, screen readback, and the drawing engine.

Algorithm

1. Set graphics window A to start at an offset of three pixels.
2. Set test window A to start at 0 (zero).
3. Draw a character at character column 22. (this causes the character to be located partly in the text window and partly in the graphics window.
4. Load the sample registers with some values (actual value is not important).
5. Place a character code in the character code register.
6. Give the draw command to draw using the sample registers and character code.
7. Repeat for character position 23. Use different values for the sample registers and the character code.
8. Perform a screen readback to verify correct data.

Path Tested Video Gate Array

Index 1 A drawing command was given to the Video gate array.

Problem: The test timed-out before the drawing engine finished the command.

Actual = 8000. The operation running bit is still active.
Expected = 0. The operation running bit is inactive.
Address = The address of the drawing engine's command register.

Action: Refer to the theory of operation for the *Video Gate Array* in Section 4. Check the address data and control signals to the array. Check for opens and shorts. If no problem is found, replace the Video gate array.

Index 2 Same as *Index 1* except the target address of the character to be drawn is different.

Index 3 Same as *Index 1* except the target address of the character to be drawn is different.

Index 4 After the character has been drawn, a screen readback is performed and the data readback is tested to be correct.

Problem: The data readback did not equal the expected data.

Actual = the data readback from the screen.
Expected = the correct data that should be read back.
Address = the address of the Video gate array sample register
that is being tested for correct data.

Action: Replace the Video gate array.

TEST AREA: MANUAL SET TIME/DATE

Test Description This test area consists of the Set Time/Date routine. This routine is not a diagnostic test. It simply allows you to set the "day," "month," and "time" of the clock calendar circuitry. Refer to the *Set Time/Date* procedures in Section 5.

TEST AREA: MANUAL KEYBOARD

Circuit Overview

The Manual Keyboard area consists of a single routine that checks the electrical operation of each console key. In so doing, the keyboard, keyboard cabling, Port 0 (Channel A of the DUART), and associated circuitry are checked.

Routine 0 **MANUAL KEYBOARD TEST**

Description This routine displays a graphic representation of the keyboard/control panel. When you press a key, the corresponding screen key reverses video. Each key can be checked in this manner. As you turn the KNOB, a KNOB position indicator point appears or disappears. The ASCII and HEX values of the pressed key and KNOB are displayed on the bottom of the graphic display.

Exit the manual keyboard test by pressing the F8 Function Key.

NOTE

For some early versions of diagnostic software you must enter Control Z to exit the Manual Keyboard test.

Path Tested Keyboard and control panel, DUART Channel A, associated circuits.

INDEX 1: Memory is allocated for the test

Problem: Could not allocate memory.

Action: Use Filer to unload and application then try the manual keyboard test again.

TEST AREA: MANUAL FLOPPY

Circuit Overview

The floppy interface circuitry consists primarily of a Western Digital® 1770 Floppy Controller/Formatter and associated circuits. This circuitry is shown on MPU Board Schematic Sheet 10. Refer to the *Floppy Interface* description in Section 4 for a detailed explanation of circuit operation.

Test Descriptions

This test area consists of three tests that involve either special user intervention, or the use of a special test disk. These tests are:

- Floppy Disk Change Test: requires technician to install/remove a "scratch" disk.
- Floppy Write/Read Test: requires use of a "scratch" disk.
- Floppy Alignment Test: requires use of the DYSAN® Digital Diagnostic Diskette.

The *Floppy Area* (described earlier in this section) five additional floppy circuit tests. The *Floppy Area* tests run automatically at power up (or can be manually selected. Once initiated, they do not require special user intervention or the use of a special test disk. Refer to *Floppy Area* earlier in these test descriptions.

Routine 0: **FLOPPY DISK CHANGE TEST**

Description: Tests the operation of the DISK CHANGE signal from the floppy drive. Prior to running this test, you must insert a "scratch" disk into the disk drive. After you initiate the test, display messages instruct you to remove and re-install the disk.

Algorithm:

1. Initiate the Restore command.
2. Step the read/write head to ensure that the DISK CHANGE signal gets set high. (The DISK CHANGE signal is set low by removing a disk. After installing a disk, the DISK CHANGE signal is set high by stepping the read/write head.)
3. Test for DISK CHANGE signal high (disk is installed).
4. Instruct user to remove and the re-install the disk.
5. Test that the DISK CHANGE signal is set low, following removal of disk.
6. Initiate Restore command. (This steps the head, causing the DISK CHANGE signal to reset high).
7. Test that DISK CHANGE signal is set high (disk is installed).

Path Tested: Checks the DISK CHANGE signal path from floppy drive to J170, pin 2, through the floppy disk control latch to IOD 00] data line. (The bit is read from address 844C01, bit 0.)

Index 1: A Restore command was given.

Problem: The restore command returned an error code. (the actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 2: Seek to Track 2.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 3: Test that the DISK CHANGE signal is high (disk installed).

Problem: Expected data (DISK CHANGE bit address 844c01 bit 0) = 0

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is high. If high, replace U260.

If the DISK CHANGE signal is not high at the above two test points, then the signal is bad from the disk drive.

Index 4. Prompt the user to remove and re-install the disk cartridge, then check that the DISK CHANGE signal goes low.

Problem: Expected data (DISK CHANGE signal address 844c01 bit 0) = 1.

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is low. If low, replace U260.

Index 5: A restore command was given.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 6: Test that the DISK CHANGE signal is high (disk installed). (The Restore command, initiated after the disk was re-installed, caused the signal to return high.)

Problem: Expected data (DISK CHANGE signal address 844c01 bit 0) = 0.

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is high. If high, replace U260.

If the DISK CHANGE signal is not high at the above two test points, then the signal is bad from the disk drive.

Routine 1: **FLOPPY WRITE/READ TEST**

Description: Writes data to the first sector on each track, then reads it back to verify data. Even-numbered tracks are tested on side 0; odd-numbered tracks are tested on side 1. Testing every other track on both sides checks all head positions and checks both sides of the disk.

Before you initiate this test, install a "scratch" disk into the disk drive.

Algorithm:

1. Allocate memory for the read/write buffer.
2. Initiate the Restore command.
3. Seek to the desired track.
4. If odd track, select side 1, else select side 0.
5. Write track number to selected track; sector 0 for side 0, or sector 5 for side 1.
6. Repeat Steps 3-5 until last track is written.
7. Seek to desired track for read.
8. If odd track, select drive 1, else select side 0.
9. Read from selected track; sector 0 for side 0, or sector 5 for side 1.
10. Check for correct read data.
11. Repeat Steps 7-10 until last track is read.

Path Tested: Checks the WRDATA (Write Data) signal from pin 22 of the controller/formatter to J170, pin 22.

Checks the WGATE (Write Gate) signal from pin 21 of the controller/formatter to J170, pin 24.

Checks the STEP signal from pin 16 of the controller/formatter to J170, pin 20.

Index 1: The system call "allocMem( )" is used to allocate RAM space for one sector of disk read/write data.

Problem: System call "allocMem( )" failed. (The actual data = the operating system error code.) Failure could be caused by insufficient memory.

Action: Re-boot the system and re-run the test. (Use the Free Up RAM command.)

Index 2: A Restore command was given to cause the disk to spin to operating speed and become ready.

Problem: the Restore command returned an error code. (The actual code = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 3: Use the Seek command to move to the desired track for a write operation.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 4: Write the track number to the track.

Problem: The Write command returned an error code. (The actual data = the disk error code. The address = the track on which writing occurs.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 5: Use the Seek command to move the the desired track for a read operation.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 6: Read the Track.

Problem: The Read command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 7: Check that data read from the track matches data previously written to that track.

Problem: The read data does not equal the expected data.

Action: This indicates that the write head is bad. If the disk was at the wrong track, or the wrong side was selected, a RECORD NOT FOUND error would have occurred during the write operation.

For additional troubleshooting information refer to *General Troubleshooting* under *Floppy Area*. If needed, refer to the *Floppy Interface* description in Section 4 of this manual and to the *Floppy Disk Drive* description in the Theory section of the applicable mainframe service manual.

Routine 2: FLOPPY ALIGNMENT TEST

DESCRIPTION

The Floppy Alignment Routine uses the Dysan® Digital Diagnostics Disk (Model #305-400) to check the alignment, centering, and spindle speed of the Floppy Disk Drive. This routine gives three types of failures; soft failures, hard failures, and system failures. From a failure indication you can make a determination as to whether the Floppy Drive or associated controller/formatter circuits are operational.

For example, if you are experiencing problems such as losing data, or reading/writing data, exercising the Floppy Alignment Routine can help further isolate the problem to either the Floppy Drive or to floppy controller/formatter circuitry on the MPU board.

CAUTION

Before you exercise the Floppy Alignment tests, select and run Floppy Routines 0 and 1, ensuring they pass before inserting the Dysan disk into the Floppy Drive. A damaged Floppy Drive Unit could damage/destroy the Dysan disk.

Activating the Test

The Floppy Alignment Routine is selected the same as any other Diagnostic routine. You can insert the Dysan Diagnostic Disk either before or after you select the test routine. After you have selected the test and inserted the disk, active the routine by pressing the "x" key. the alignment tests run automatically.

Test Sequence

After you press the "x" key, the alignment routines run automatically. Three tests are run:

1. Floppy Drive Centering test
2. Floppy Drive Alignment test
3. Spindle Speed check

These tests are run sequentially. As they are run, the display shown in Figure 9-3 is developed. This figure shows how the display appears at the conclusion of the alignment routine. This display shows the results of each test. Refer to the following individual test descriptions for information on how to interpret the test display.

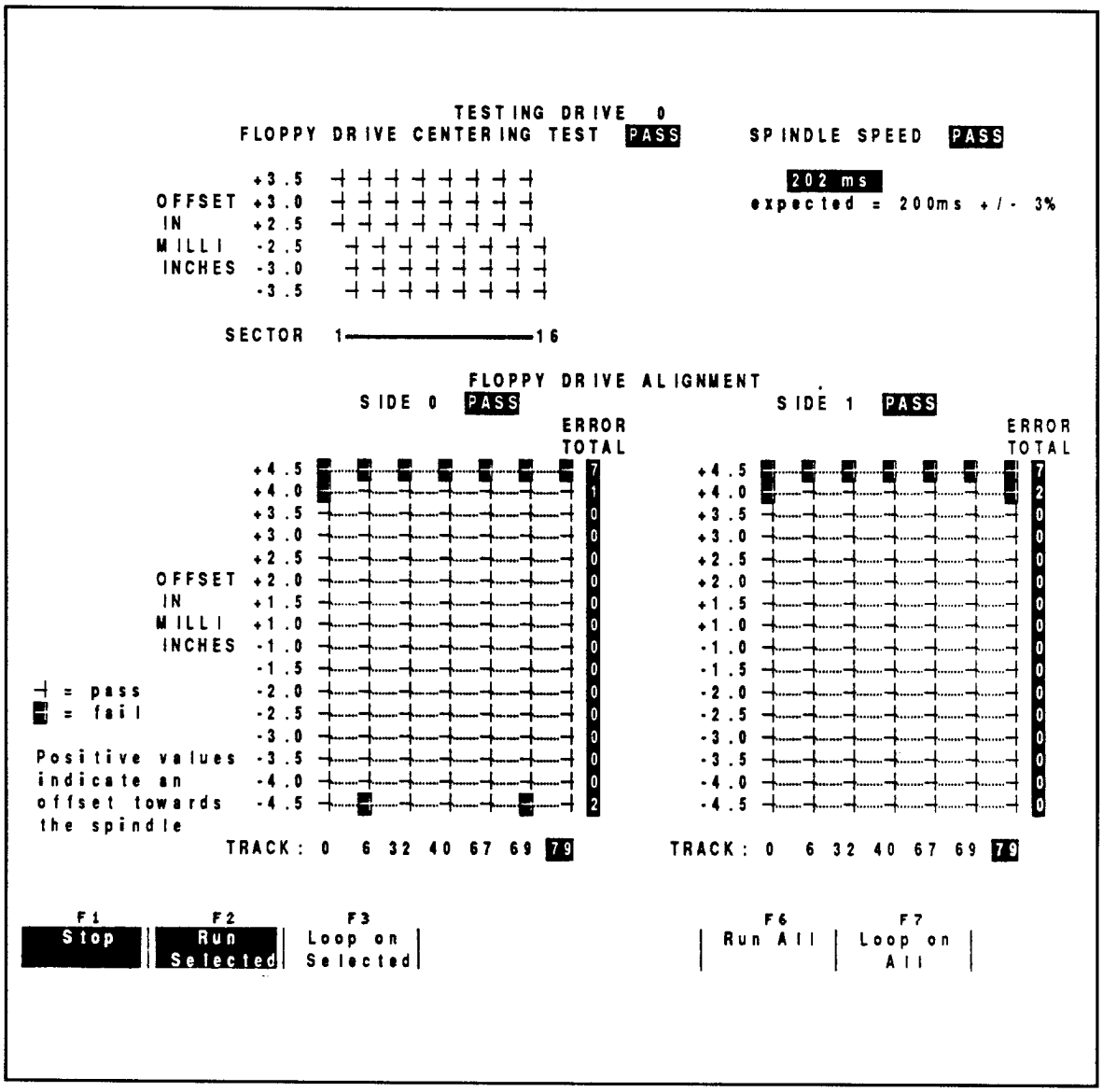


Figure 9-3. Floppy alignment routine display.

Floppy Drive Centering Test

A centering track is read from the Dysan disk. This track contains 16 sectors of data that are each 3.0 mil inch off-center. Each track has a different offset: track 1 is offset +/- 2.5 mil inch, track 2 is offset +/- 3.0 mil inch, and track 3 is offset +/- 3.5 mil inch. The odd-numbered sectors are offset +2.5 mil inch and the even sectors are offset -2.5 mil inch. The track is read off the disk and plotted on the screen as each sector is read.

Interpreting Test Results. A failure is indicated by a solid fill in an "off-set" rectangle. A drive that is off-center will cause failures at both the + and - offsets. Failures at only the + or - offset may indicate the drive is out of alignment. Refer to *Floppy Drive Alignment Test* description below. Refer also to *Alignment Failures* which follows, for additional information. Centering is considered good if the drive passes the +/- 2.5 and +/- 3.0 mil inch offset tests.

Floppy Drive Alignment Test

Refer to Figure 9-3. Both sides of the Dysan Disk contain data on several progressively-offset tracks. The sectors for each track (16 tracks per sector) contain offset data starting at +1 mil inch at Sector 1, -1 mil inch at Sector 2, then progressing in .5 mil inch increments until Sector 15 = +4.5 mil inch, and Sector 16 = -4.5 mil inch. This offset pattern is illustrated in the alignment display shown in Figure 9-4. Note that both sides of the disk are checked.

Interpreting Test Results. A track alignment failure is indicated by a solid fill in an off-set rectangle. For example, Figure 9-3 shows that all even-number tracks on both sides of the disk had read failures at the -4.5 mil inch offset. A positive offset indicates an offset toward the spindle; a negative offset indicates an offset away from the spindle. Refer to *Alignment Failures* below, for additional information.

The point where a floppy drive alignment graph shows failures indicates the degree to which the drive is out of alignment. For example, most drives cannot read data offset greater than 4.0 mil inch. However, if the graph shows read failures less than + or - 2.5 mil inch, the floppy drive is too far out of alignment and should therefore be replaced.

Alignment Limit Test

This test determines if the floppy drive is operating within specified limits. If this test fails the alignment limits, then a "FAIL" message flashes on the display next to the test name. If this test passes, then "PASS" is displayed following the test name. If the test fails a read outside of the specified limits of the drive, the test passes. The test fails only if it fails a read inside the specified limits of the drive. For example.

1. Disk drive is good if test can read a disk with an offset up to +/- 3.0 mil inch. Disk drive is good as long as Read failure is due to an offset greater than 3.0 mil inch.
2. If test fails to read an offset of 3.0 mil inches and below, then disk drive is bad.

Refer to *Indexes 6* through *9*.

Spindle Speed Test

This test obtains five samples of spindle speed, averages them, and prints the spindle speed in msec per rotation.

Interpreting Test Results. Spindle speed for the Floppy Drive unit is specified at 200ms ± 6 ms per revolution. Figure 9-3 indicates spindle speed is within specified limits.

Alignment Failures

The Floppy Alignment Routine indicates three kinds of failures: soft failures, hard failures, and system failures.

Alignment failures occur when the offset data cannot be read back from the DYSAN diskette. As described earlier, the alignment test is plotted on a displayed graph. The drive is considered in alignment if it passes offsets of 0.003-inch and under. Disk drives are considered acceptable if failures occur above ± 0.003-inch.

Hard Failures. Hard failures stop the Floppy Alignment Routine. Hard failures occur when the floppy controller/formatter IC (located on the MPU board) reports an error other than a read error. For example: hard failures would occur if the Floppy Drive could not seek to the specified track, could not find the sector, or it lost data.

NOTE

A drive that is excessively out of alignment will cause a hard failure.

A hard failure indicates a serious problem; usually with the Floppy Drive, although hard failures can occur if there is a serious problem with the floppy controller/formatter circuitry. Controller/formatter problems should first be troubleshot using the other floppy diagnostic routines.

Hard failures are displayed as a flashing "DRIVE ERROR" message inside the graph currently being drawn.

Action Following A Hard Failure. If the Floppy Alignment Routine displays a "DRIVE ERROR" message, press the STOP special function key. The data that then appears is the actual disk failure code. Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 1: System memory is allocated.

Problem: System could not allocate memory

Action: Use the FILER menu to free up system RAM, then try again.

Index 2: The Restore command was given to the drive.

Problem: The Restore command returned an error. The actual data = the disk error code.

Action: Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 3: The model number is read from the Dysan disk.

Problem: A read error occurred when the disk was read.

Action: Check to ensure the Dysan disk is installed. Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 4: A hard error occurred during one of the tests.

Problem: The actual data = the disk error code.

Action: Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 5: During the Spindle Speed test, the floppy formatter/controller could not detect the index pulse.

Problem: Floppy.controller/formatter cannot detect the index pulse.

Action: Loop on test. Check for a pulse on pin 24 of U250 (the Western Digital Floppy Controller/Formatter IC).

TEST AREA: MANUAL DISPLAY

Circuit Overview

This area consists of one test that checks the operation of the display controller circuitry that drives the color CRT monitor or the flat panel display.

Routine 0 **DISPLAY TEST**

Description This test first checks to determine what type of display is attached to the mainframe. If a color CRT is attached, the test algorithm prompts you to press a key to display a full screen of color bars. You must press another key to exit the color bars test.

If a flat panel display is attached, the algorithm prompts the technician to press a key to obtain one of nine test patterns.

Algorithm

1. If color crt monitor is installed, prompt the user to press a key to display color bar pattern. (User must press a keyboard key to exit the test.)
2. If flat panel display attached, prompt user to press a key to begin sequence of display patterns.

The user can press any key to sequence through the following series of flat panel tests patterns:

a. All on. Check that all pixels are lighted.

b. All off. Check that all pixels are off.

c. Vertical Lines, 2 on/2 Off. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

d. Vertical Lines, 2 Off/ 2 ON. Check for shorted lines; that is, only two adjacent lines turn on. A short causes three or more adjacent lines to be on.

e. Horizontal Lines, 2 On/2 Off. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

f. Horizontal Lines, 2 Off/2 On. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

g. Checkerboard. A checkerboard pattern is displayed. Check for shorted pixels. No adjacent pixels should be lighted.

h. Vertical Scroll. Check for flicker and/or lit pixels, other than those that comprise the smooth-scrolling vertical bar.

i. Horizontal Scroll. Check for flicker and/or lit pixels other than those that comprise the smooth-scrolling horizontal bar.

j. Exit test patterns when key is pressed following display of last test pattern (horizontal scroll).

Path Tested

Display video data and control signal paths from Video gate array and RAM to and from the attached display unit.

Index 1

Problem: Could not allocate memory.

Actual = System error code.
Expected = 0
Address = zero (0) has no meaning

Action: To free-up RAM, use the Filer menu to unload an application, then re-run the test..

TEST AREA: MANUAL CLOCK ADJUST

Test Description

This test area consists of the *Clock Adjust* routine. This routine is not a diagnostic test. It is used to make an accurate adjustment of the Calendar oscillator frequency. Refer to the *Set Clock* procedures in Section 5, *Adjustments.*

NOTE

If the Set Clock routine does not work, verify operation of the calendar circuits by running routines 0, 1, and 2 of the Clock Test Area.

TEST AREA: MANUAL MODULE ID

Test Description

This test can be used as an aid to troubleshoot suspected acquisition module communication problems. This test always passes and therefore has no failure indexes. To run the test, perform the following steps:

1. Select the Manual Module ID diagnostic test.
2. Press the F2 key. The display prompt will ask for the number of the module to be tested.
3. Enter the number of the desired module to be tested. Numbers 0-7 correspond to modules inside a mainframe while numbers 8-F correspond to expansion mainframe modules. (Most mainframes use only module ID numbers 0 and 1.)
4. After you enter the module ID number, the test will run in a continuous loop. To obtain the results, press the F1 (stop) key.

A successful module ID will display the following information:

Address	Expected	Actual	Index
The module ID no. (0-8 Internal module, 8-F External module)	The module ID no. (0-8 Internal module, 8-F External module)	The module ID no. (0-8 Internal module, 8-F External module)	D00

An unsuccessful module ID will display the following information:

Address	Expected	Actual	Index
The module ID no. (0-8 Internal module, 8-F External module)	FFFF	FFFF	D00

Any unsuccessful module ID tests indicate a missing module, incorrectly configured system, or a TekLink hardware communication problem.

Hard Disk Module Test Descriptions

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU board) Module, ROM, and Even Rom C/S are selected. If you enter Diagnostic Mode and select the Hard Disk module, you see the hard disk circuit areas that are tested. The module test descriptions are presented in the order as listed on the display.

Refer to Section 4, *Theory of Operation*, in the applicable mainframe service manual for a detailed description of Hard Disk Controller or IDE Interface board and Hard Disk Drive operation. Refer to Section 10, *Diagrams*, in the applicable mainframe service manual for a detailed block diagram, signal interconnect diagrams, and schematics.

The following descriptions for the hard disk drive diagnostic tests apply to both types of hard drive interfaces that can be used with the MPU board. The two types of hard disk drive interfaces are ST506/412 and IDE (AT). The diagnostic software determines the type of hard disk drive installed and calls the appropriate tests for the drive type.

The Hard Disk test module for the ST506/412-interface drive consists of three tests:

1. Hard Disk Memory and Controller
2. Hard Disk Read and Write
3. Hard Disk Format

The Hard Disk test module for the IDE-interface drive consists of two tests:

1. Hard Disk Diagnostics
2. Format

NOTE

If the hard disk drive is replaced, format the drive before exercising the Hard Disk module diagnostic tests. Refer to Hard Disk Format *area for instructions on how to format a hard disk.*

TEST AREA: HARD DISK MEMORY AND CONTROLLER

Circuit Overview

This set of four routines tests the operation of WD2010, hard disk RAM, and associated circuits for a ST506/412-interface hard disk drive. Refer to Section 10, *Schematics*, of the applicable mainframe service manual for a detailed block diagram and schematics. Also see Section 4, *Theory of Operation,* this manual, for a detailed explanation of circuit operation.

Test Descriptions

The hard disk memory and controller area is verified by the following tests:

- Hard Disk Controller Registers test
- Hard Disk Memory Data-line independence test
- Hard Disk Memory Address-line independence test
- Hard Disk CMOS RAM parts integrity test

Routine 0 **HARD DISK CONTROLLER REGISTERS**

Description Checks five controller registers in the WD2010 (U340). The five registers and their addresses are:

REGISTER	ADDRESS
Sector Count	850005
Sector Number	850007
Cylinder Low	850009
Cylinder High	85000B
SDH register	85000D

The sector count register is tested by writing to it eight times and reading from it eight times. All others are tested by writing to them twice each and reading from them twice each.

Algorithm

1. Write to the sector count register with a "walking 1-bit." Read back the register to verify that same byte is returned. Repeat this process eight times.

2. For all other registers except cylinder high register, write AA in hex code and read back for verification. Next, write 55 in hex code and read back for verification.

3. For cylinder high register, write 02 in hex code and read back for verification. Next, write 05 in hex code and read back for verification.

Path Tested: WD2010 registers, U19, U20, and U21 data transceivers, U330 decode PAL (CREG/) and U220 timing PAL (WECTC/ and RECTC/).

Index 1 Readback data from register address 850005 hex. Actual data is the readback data. Expected data is the "walking 1-bit" pattern written to the register.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check WD2010 controller U340
- Check data transceivers U19, U20, U21
- Check CREG/ at decode PAL U330
- Check WECTC/ and RECTC/ at timing PAL U220

Index 2 Two write/read cycles are performed on the sector number register, address 850007 hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 3: Two write/read cycles are performed on the cylinder low register, address 850009 hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 4:

Two write/read cycles are performed on the cylinder high register, address 85000B hex. The first byte written is 02 hex. The second byte written is 05 hex. Expected data from the first readback is 02 hex. The second expected readback data is 05 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 5:

Two write/read cycles are performed on the SDH register, address 85000D hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Routine 1 **HARD DISK MEMORY DATA LINE INDEPENDENCE TEST**

Description

This test checks data lines DC[0:15] of the hard disk RAM and associated circuitry. The 68010 microprocessor, on the MPU board, uses two address locations for this test: 850000 hex for the hard disk buffer register, and 850011 hex for the hard disk control register.

The test first sets the hardware (address counter) to zero. This is done by writing 06 hex then 66 hex (in that order) to the hard disk control register (850011). It then writes a sequence of 2-byte words (one word after another) to the hard disk buffer register (850000).

NOTE

This test should be run prior to the address line independence test (routine 2). The address line test depends on good data lines; whereas, the data test doesn't need a perfectly working address line.

Algorithm

1. Set "actual" data to zero.
2. Repeat the following 6 steps for each possible data word.
3. Reset the hardware counter to zero.
4. Write a word (2 cycles) to the hard disk buffer register.
5. Reset the hardware counter to zero.
6. Read a word (2 cycles) from the hard disk buffer register.
7. Exclusive OR the written word with the read word.
8. OR the result with the "actual" data and write the result back to "actual".

Path Tested

Tests the data transceivers (U19, U20 and U21), RAM (U140 and U150), control signals CLRCTR, CS/, CSIDHRAM/, OE/, DE/, and clock from decode PAL (U330); plus WE/ and WECTC/ from timing PAL (U220). The address counters (U350 and U130) are tested for reset capability.

Index 1

Test data lines DC[0:15].

Problem: One or more 2-byte words of data written to the hard disk buffer memory were read back differently. When exclusive ORed, the bad data will show as a one. Expected data is for all lines (0:15) to be zero. Invoke the expansion text (press the NOTES key) to get a list of the bad data lines. Bit 0 corresponds to line 0, bit 1 to line 1, etc.

Action: If all data lines failed, check cable J390.

If there are problems with data lines 0:7 only and test routine 0 passed, then check U140.

If there are problems with data lines 8:15 only and test routine 0 passed, then check U150.

If there are problems with any of the data lines, check the following:

- Data transceivers U19, U20, U21
- Decode PAL U330
- Timing PAL U220
- Address counters U1 and U130 (for reset function)

Routine 2 **HARD DISK MEMORY ADDRESS LINE INDEPENDENCE TEST**

Description Tests the address counter, address lines AC[0:12] and associated circuitry. Test is performed by writing the address number into RAM at the corresponding address location. The data read back should be the same as the address location from which it was read.

NOTE

This test should be performed only after routine 1 has passed. Any problems with the data bus or registers results in an error from this tests.

Algorithm

1. Reset the hardware counter to zero. This is done by writing 06 hex, then 66 hex to the 68010 address location 850011.
2. Repeat the following step for each possible address.
3. Write a word (the current address number) to the hard disk buffer register. The 68010 address for the hard disk buffer register is 850000 hex.
4. Set "actual" data to zero.
5. Reset the hardware counter to zero.
6. Repeat the following three steps for each possible address.
7. Read a word from the hard disk buffer register.
8. Exclusive OR the read word with the expected address.
9. OR the result with the "actual" and write the result back to "actual".

Path Tested U120 (AC 0), U130 (AC[1:8]) and U350 (AC[9:12]). Also checks input of U140 and U150 (RAM). Control signals from the decode and timing PALs plus gates/flip-flops U10, U16, U22, U18 and U24.

Index 1

Test address lines AC[0:12].

Problem: One or more of the 2-byte words of data (address values) written to the hard disk buffer memory were read back differently. The 13 least-significant bits correspond to the 13 address lines, AC[0:12].

After read data and expected data (address value) are exclusively ORed together, all resulting bits should be zero. Any bits that are set to a "1" value indicate a problem with that address location. Invoke the expansion text (FB key) to get a list of the bad address lines.

Action: Check the first bad address reported and note its most significant bit (MSB). For example, if only AC[12], AC[11] and AC[10] addresses are reported as bad, check AC10 for a short to ground.

NOTE

The address lines are driven by hardware counters. If one address line is grounded., the next higher lines never get the carry and consequently appear defective.

If AC0 is reported bad, check to see if it is shorted with another line. AC0 is unique. If it is shorted with another line, it will take on the value of the other line.

If just two addresses are reported bad, check to see if they are shorted together. If one line failed, check it for shorts or opens.

Other circuits to check are: U140 and U150 (RAM), U120 (AC0), U130 (AC[1:8]) and U350 (AC[9:12]).

Also check control signals from U330 (decode PAL) and U220 (timing PAL) plus gates/flip-flops U10, U16, U22, U18, and U24.

Routine 3 **HARD DISK CMOS RAM PARTS INTEGRITY TEST**

Description This is a test of the integrity of the CMOS RAM and associated circuitry. This test is similar to routine 1 except that it tests all 8192 address locations of the RAM.

NOTE

This test should be run only after routines 1 and 2 have passed. If there is any problem with the data or address buses, this test will result in erroneous information.

Algorithm

1. Reset the hardware counter to zero. This is done by writing 06 hex then 66 hex to the MPU's 68010 address 850011.
2. Set "actual" data to zero.
3. Repeat the following step for each possible address.
4. Write FFFF to the hard disk buffer register. The MPU's 68010 address for this is 850000 hex.
5. Reset the hardware counter to zero.
6. Repeat the following three steps for each possible address.
7. Read a word from the hard disk buffer register.
8. OR the "actual" data with the logical "not" of the read word.
9. Write the above result back to "actual".
10. Repeat the following step for each possible address.
11. Write 0000 hex to the hard disk buffer register.
12. Reset the hardware counter to zero.
13. Repeat the following three steps for each possible address.
14. Read a word from the hard disk buffer register.
15. OR the "actual" data with the read word.
16. Write the above result back to "actual" data.

Path Tested Data transceivers U19, U20, U21 and control signals from U330 decode PAL, U220 timing PAL. Address counters U350, U120 and U130 plus RAM chips U140 (DC[0:7]) and U150 (DC[8:15]). Also tests gates/flip-flops U10, U16, U22, U18 and U24.

Index 1

Test memory cell bits [0:15] for every address.

Problem: One or more 2-byte words of data written to the hard disk buffer memory were read back differently. The "actual" data is a 16-bit word. Bit 0 of "actual" data represents data cell 0 of RAM, bit 1 represents cell 1 and so forth. When ORed with the data (or not data) read back from memory, the result should be that all bits are zero. A set bit (logic "1") indicates a bad data cell.

Action: If routines 1 and 2 have already passed, then the problem is with RAM. If any bit from 0:7 is bad, then check U140. If any bit from 8:15 is bad, then check U150.

NOTE

The two least significant hex numbers of "actual" data represent bits 0:7 of RAM and the two most-significant hex numbers represent bits 8:15 of RAM.

TEST AREA: HARD DISK READ AND WRITE

Circuit Overview

The hardware being tested consists of the Hard Disk Controller board and the ST506/412-type, half-height, rigid-media, disk drive.

Routine 0 **TEST WRITE AND READ TO/FROM HARD DISK**

Description This routine writes a 1K file to the hard disk. The file is read back and verified.

Algorithm

1. Create directory, tmp_dir (if one does not already exist).
2. Open file </hard disk/tmp_dir/tmp_file> for writing.
3. Write to the file 1K of data consisting of the following:
   256 bytes of 55 hex
   256 bytes of AA hex
   256 bytes (0 through 255 in scrambled order)
   256 bytes (same as previous 256 bytes)
4. Close the file.
5. Reopen file for reading.
6. Read file and verify that data is correct.
7. Close the file.
8. Remove the file.
9. Remove the directory if created by this test.
10. Report results of test.

Path Tested Hard Disk Controller board and the ST506/412-type, half-height, rigid-media disk drive.

Index 1

Test write and read to/from the Hard Disk.

Problem: The operating system returned an error code when this routine called one of the file system interface routines, or one or more bytes of data did not verify upon readback. The expected data is zero. The address is zero.

The actual data is a 16-bit word with the least-significant hex number encoded to convey the following:

- Bit 0: One or more of the 55 hex bytes did not verify.
- Bit 1: One or more of the AA hex bytes did not verify.
- Bit 2: One or more of the random bytes did not verify.
- Bit 3: One or more of the file system interface outines returned an error code.

Action: If only bit 3 is set and if Hard Disk Memory and Controller test area routines passed, then check cables J400, J200, J390 and J190. Also check to see if you can manually create /hard disk/tmp_dir, and check if there is 1K available on the hard disk.

If only bit(s) 0 through 2 are set, try using another hard disk drive.

If bit 3 and some other bit(s) are set, verify that there is 1K available on the disk then try another hard disk drive.

NOTE

No attempt is made to write to the disk unless /hard disk/tmp_dir can be made or its existence verified. If one or more of the bits from 0 through 2 is set, then some functionality exists. If so, cabling is probably not a problem.

TEST AREA: HARD DISK FORMAT

Circuit Overview

This test area consists of a single routine that formats a ST506/412-interface hard disk drive.

Routine 0 **FORMAT**

Description

Use this routine to format a hard disk. As part of the format routine, you must enter the disk manufacturer's bad block data under the following circumstances:

- Whenever the installed disk or any hard disk controller circuitry have been repaired.
- Whenever the failure and repair of other system failures may indicate the disk needs to be reformatted.

NOTE

Reformatting under the above two circumstances frees-up bad blocks that may have been entered into the disk's bad block table as a result of the hardware problem.

- Whenever a new disk is installed.

Bad block data for a currently installed hard disk is located on a label on top of the hard disk drive. Bad block data for a replacement hard disk unit is located on a label stuck to the hard disk drive unit.

Instructions on when and how to enter the data are provided on the display screen as the routine is exercised.

NOTE

Enter only the cylinder/head information listed on the label.

At the completion of the routine, the total number of bad blocks is displayed at the top of the display screen. If this number exceeds 100, either the disk drive unit or controller circuitry have failed. Contact your Tektronix service representative for assistance.

Algorithm

The hard disk Format routine performs the following sequence:

1. Obtain the bad block table.
2. If no bad block table, prompt the user for manufacturer's bad block information.
3. If bad block table exists, prompt the user to re-enter to re-enter that bad block table (see description above for the two circumstances under which user should re-enter bad block information).
4. Format the disk.
5. If user entered the manufacturer's bad block table information, add the entered data to the bad block table created by the format routine. (The format routine adds bad blocks to the table if it encounters them while formatting the disk.)

If user declined to re-enter the manufacturer's bad block data, then add the old bad block table to the new bad block table.

Path Tested

Hard Disk Controller circuits and hard disk drive unit.

Index 1

Memory is allocated for the bad block table.

Problem: System could not allocate memory.

Actual:	82 = not enough system memory. 83 = no free segments. 96 = system timed-out waiting for free memory.
Expected:	0
Address:	not applicable.

Action: Use the Ram Operations menu to unload an application from RAM (to free memory) and exercise routine again.

Index 2

An attempt was made to format the disk.

Problem: A non-recoverable error occurred when trying to format the disk. The error could be caused by bad media on cylinder 0, heads 0, 1, or 2, or by an electrical problem with the hard disk drive or controller circuitry.

Actual: 340 = System error code for bad media on system disk.
Expected: 0
Address: not applicable.

Action: Troubleshoot and repair the hard disk controller circuitry as required (Run other Hard Disk diagnostic routines). Replace the hard disk drive.

Index 3

Add the old bad block information, or the recently-entered manufacturer's bad block data, to the bad block table.

Problem: A non-recoverable error occurred when trying to add to the bad block table. The error could be caused by bad media on cylinder 0, heads 0, 1, or 2, or by an electrical problem with the hard disk drive or controller circuitry.

Actual: 359 = system error code for illegal bad block entry (cylinder 0, head 0, 1, or 2)
344 = system error code for device error, signifying an electrical problem with the hard disk drive or controller circuitry.
Expected: 0
Address: not applicable

Action: Replace the Hard Disk Unit.

TEST AREA: HARD DISK DIAGNOSTICS

Circuit Overview

This diagnostic test initiates an internal diagnostic test of the controller circuitry in an IDE-interface hard disk drive. A correctly operating IDE Interface board is needed for this test to execute. Refer to *Section 10, Diagrams* in the appropriate mainframe service manual for a detailed schematic diagram of the IDE Interface board. Also see *Section4, Theory of Operation* in the same manual for a description of the circuit operation.

Test Description

This test issues a single command to the IDE-interface hard disk drive. This command causes the hard disk drive to execute a set of internal diagnostics tests for drive. The tests verify proper operation of the formatter device, sector buffer, ECC circuitry, and controlling microprocessor that are part of the hard disk drive.

Error Reporting

The results of the internal diagnostic tests for the hard disk drive are available for display on the Diagnostic menu. To view the results, move the cursor to the Routine field. Use the Help Notes key to display the results.

If the routine was not executed, the message is:

```
The hard disk diagnostics routine has not been executed.
```

If the routine executed without errors, the message is:

```
The hard disk diagnostics routine was executed and found no
errors.
```

If the routine executed and an error was detected, the message is the following paragraph with one of the four error strings listed below the paragraph:

```
The hard disk diagnostics routine was executed and the error
noted below was found.  The hard disk is not operating
correctly.  Any operation performed on the disk may corrupt
existing data.  Data read from or written to the drive may be
corrupt.

Formatter device error.

Sector buffer error.

ECC circuitry error.

Controlling microprocessor error.
```

TEST AREA: HARD DISK FORMAT

Test Description

This test consists a single routine that formats the IDE-interface hard disk drive. The routine automatically reads the necessary parameters from the Identify Drive registers of the hard disk drive. The routine then starts formatting the hard disk drive with no interaction with the user. When the routine is completed and no errors occur, the following message is displayed:

```
Hard disk format completed successfully.  #1 bad blocks found –
#2 before.
```

Where #1 is the number of bad blocks found during the formatting process and #2 is the number of bad blocks marked before the process.

Error Reporting

The results of the format routine for the hard disk drive are available for display on the Diagnostic menu. To view the results, move the cursor to the Routine field. Use the Help Notes key to display the results.

If the routine has not run, the message is:

```
The hard disk diagnostics routine has not been executed.
```

If the routine executed without errors, the message is:

```
The hard disk format routine successfully format the hard disk.
```

If the routine executed and an error was detected, the message is:

```
The hard disk format routine could not successfully format the
hard disk drive.  The boot sector could not be updated.  Any
data remaining on the hard disk may be corrupted.  Run the hard
disk diagnostics for more information. ECC circuitry error.
```

1200C01 COMM Pack Module Tests

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU board) Module, Manual Floppy Area, and test Routine 2 are selected. If you enter Diagnostic Mode and select the d1200C01 module, you will see the COMM pack circuit areas that are tested. The d1200C01 module test descriptions are presented in the order as listed on the display.

TEST AREA: RS232

Circuit Overview

COMM pack Interface circuits are shown on MPU Board Schematic, Sheet 4. Refer to the *Communications Pack Interface* descriptions in Section 4 for a detailed explanation of circuit operation.

Test Description

The RS232 COMM pack interface is tested using the following diagnostic routines:

- Internal Loopback test
- External Loopback test

Routine 0: **UART INTERNAL LOOPBACK TEST**

Description: COMM pack is set to local mode and a data string is transmitted internally.

Algorithm:

1. Read the COMM pack identification to check if a COMM pack is installed.
2. Disable the 8250 interrupts.
3. Put the 8250 in Internal Loopback mode.
4. Test for cleared status register
5. Enable the transmitter.
6. If status register = "transmitter ready," send a character.
7. If status register = "receiver ready," read a character.
8. Repeat Steps 6 and 7 until the last character in the test string is transmitted or an error occurs.

Path Tested: U220 (COMM pack's 8250 UART), U126, and U116.

Index 1 After the UART is initialized, the status register is checked for clear.

Problem: Status register was not cleared.

Action: Replace U220.

Index 2 After the UART is initialized, the modem status register is checked for clear.

Problem: Status register was not cleared.

Action: Replace U220.

Index 3 The transmitter is enabled and checked for ready.

Problem: The transmitter was not ready.

Action: Replace U220.

Index 4

The transmitter shift and holding registers tested empty.

Problem: One register or the other was not empty. Bit 5 = 1 = holding register empty. Bit 6 = 1 = shift register empty.

Action: Replace U220.

Index 5

A character was received and the status register is checked for errors.

Problem: Status register indicated an error.

Action: Replace U220.

Index 6

The test reads the COMM pack Identification.

Problem: The read action did not read an identification. COMM pack may not be installed.

Action: Ensure the COMM pack is installed. If installed, check the CROM(L), COMM(L),, IRD(L), and IWR(L) signals. If OK, replace ROM, U126.

Index 7

The received string is compared against the transmitted string.

Problem: The received string did not match the transmitted string.

Action: Replace U220.

Routine 1: **HOST EXTERNAL LOOPBACK TEST**

Description: Performs an external loopback test on the COMM pack. Requires that an external loopback connector be connected to the COMM pack's external connector. (The loopback connector has pin 2 (TRANDATA) connected to pin 3 (RECDATA) and pin 5 (CTS) connected to pin 20 (DTR).

Algorithm:

1. Set a pointer to the COMM pack's get_char( ) and put_char( ) routines.
2. Initialize the transmit_string.
3. Send a character.
4. Test to see if the UART received the character.
5. If character was received, read and save the character.
6. Repeat 3-6 until end of string or timed out.
7. Test that the received string equals the transmit string.

Path Tested: Tests the following signals from the 8250 UART (U220) to the COMM pack's host connector: RD, TD, CTS, DTR. Also tests the COMM pack interrupt signal, COMPKIRQ.

Index 1: A character is transmitted and the COMM pack receiver is checked to see that it received the character. If no character is received before a time-out, this test fails.

Problem: The UART did not receive a character.

Action: Run the Host Internal Loopback test (Routine 0). If it passes check the TD/RD path from TD pin 11 of the UART to pin 2 of the loopback, back through pin of the loopback connector , to RD pin 10 of the UART.

Index 2: The UART detected an error after a character was received. The UART's status register is examined and the test index number is set accordingly.

Problem: Overrun error - caused when the receiver buffer overflows.

Actual = 010H

Index 3: See description for *Index 2.*

Problem: Parity error - caused when a character is received with the incorrect parity bit.

Actual = 20H

Index 4: See description for *Index 2.*

Problem: Index 4 - framing error - caused by no stop bit received.

Actual = 40H

Index 5: See description for *Index 2.*

Problem: Received break - caused when an all zero character was received without a stop bit.

Actual = 80H

Index 6: See description for *Index 2.*

Problem: A combination of the above errors. Example: Actual = 30H means an overrun and a parity error.

Action (for Indexes 2-6): Check the TD/RD path (from TD pin 11 of the UART to pin 2 of the loopback connector , back through pin of the loopback connector, to RD pin 10 of the UART).

Index D Data transmitting is complete and the received string is compared to the transmitted string.

Problem: Actual does not equal expected.

Action: Check the TD/RD path (from TD pin 11 of the UART to pin 2 of the loopback, back through pin of the loopback, to RD pin 10 of the UART).

Section 10
REPLACEABLE ELECTRICAL PARTS

Parts Ordering Information

Replacement parts are available from or through your local Tektronix sales and service office or field representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix service center or field representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

List of Assemblies

A list of assemblies is given at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

Cross Index-Mfr Code Number to Manufacturer

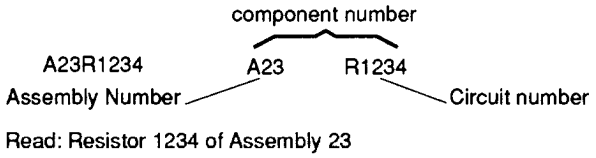
The Mfr. Code Number to Manufacturer Cross Index for the Electrical Parts List is located immediately following this format information. The Cross Index provides codes, names, and addresses for the manufacturers of components listed in the Electrical Parts List.

Abbreviations

Abbreviations in this section conform to American National Standard Y1.1.

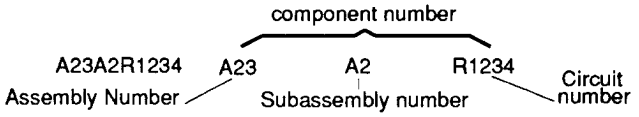
Component Number (column 1)

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

The circuit component number appears on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the mechanical parts list. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

Tektronix Part Number (column 2)

Indicates part number to be used when ordering replacement part from Tektronix.

Serial Number (columns 3 & 4)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number indicates part is good for all serial numbers.

Name and Description (column 5)

In the Parts List, an Item Name is separated from the description by a colon(:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

Mfr. Code (column 6)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

Mfr. Part Number (column 7)

Indicates actual manufacturer's part number.

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL	HARRISBURG PA 17105
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
01961	VARIAN ASSOCIATES INC PULSE ENGINEERING SUBSIDIARY	7250 CONVOY CT P O BOX 12235	SAN DIEGO CA 92112
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
08261	SPECTRA-STRIP	7100 LAMPSON AVE	GARDEN GROVE CA 92642
0JR03	ZMAN AND ASSOCIATES	7633 S 180th	KENT WA 98032
0JR04	TOSHIBA AMERICA INC	2692 DOW AVE	TUSTIN CA 92680
0KB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
11236	CTS CORP	406 PARR ROAD	BERNE IN 46711-9506
12954	MICROSEMI CORP - SCOTTSDALE	8700 E THOMAS RD	SCOTTSDALE AZ 85252
18324	SIGNETICS CORP	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
19701	PHILIPS COMPONENTS DISCRETE PRODUCTS	PO BOX 760	MINERAL WELLS TX 76067-0760
1Y013	ACACIA/DEANCO	3101 SW 153RD DRIVE	BEAVERTON OR 97006
20933	KAPPA NETWORKS INC	765 ROOSEVELT AVE	CARTERET NJ 07008
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
23875	M-TRON INDUSTRIES INC	100 DOUGLAS ST	YANKTON SD 57078-4430
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR	FRANKLIN IN 46131
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532-1613
31433	KEMET ELECTRONICS CORP	PO BOX 5928	GREENVILLE SC 29606
32997	BOURNS INC	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086-4518
34371	HARRIS CORP HARRIS SEMICONDUCTOR PRODUCTS GROUP	200 PALM BAY BLVD PO BOX 883	MELBOURNE FL 32919
34899	FAIR-RITE PRODUCTS CORP	1 COMMERCIAL ROW	WALLKILL NY 12589
4T165	NEC ELECTRONICS USA INC ELECTRON DIV	401 ELLIS ST PO BOX 7241	MOUNTAIN VIEW CA 94039
50434	HEWLETT-PACKARD CO	370 W TRIMBLE RD	SAN JOSE CA 95131
51791	STATEK CORP	512 N MAIN ST	ORANGE CA 92668-1102
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
57668	ROHM CORP	8 WHATNEY	IRVINE CA 92713
59640	SUPERTEX INC	1225 BORDEAUX DR	SUNNYVALE CA 94086
59660	TUSONIX INC	7741 N BUSINESS PARK DR	TUCSON AZ 85740-7144
61058	MATSUSHITA ELECTRIC CORP OF AMERICA PANASONIC INDUSTRIAL CO DIV	ONE PANASONIC WAY PO BOX 1502	SECAUCUS NJ 07094-2917
61271	FUJITSU MICROELECTRONICS INC	2985 KIFER RD	SANTA CLARA CA 95051-0802
61429	FOX ELECTRONICS	PO BOX 1078	CAPE CORAL FL 33910-1078
61857	SAN-O INDUSTRIAL CORP	85 ORVILLE DR	BOHEMIA LONG ISLAND NY 11716-2501
61892	NEC ELECTRONICS USA INC MICROCOMPUTER DIVISION	1 NATICK EXECUTIVE PARK	NATICK MA 01760
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
63791	STAR MICRONICS INC	200 PARK AVE	NEW YORK NY 10166-0001
64155	LINEAR TECHNOLOGY CORP	1630 MCCARTHY BLVD	MILPITAS CA 95035-7417
66302	VLSI TECHNOLOGY INC	1109 MCKAY DR	SAN JOSE CA 95131-1706
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
75378	CTS KNIGHTS INC	400 REIMANN AVE	SANDWICH IL 60548-1846
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
91637	DALE ELECTRONICS INC	2064 12TH AVE	COLUMBUS NE 68601-3632
TK1471	PHOENIX CONTACT INC	1900 GREENWOOD ST	HARRISBURG PA 17104
TK1864	INTERFET CORP	322 GOLD ST	GARLAND TX 75042

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1	672-1304-00	B010100	B010154	CIRCUIT BD ASSY:MPU	80009	672-1304-00
A1	671-0058-01	B010155	B010164	CIRCUIT BD ASSY:MPU	80009	671-0058-01
A1	671-0058-02	B010165	B010166	CIRCUIT BD ASSY:MPU	80009	671-0058-02
A1	671-0058-03	B010167	B010183	CIRCUIT BD ASSY:MPU	80009	671-0058-03
A1	671-0058-04	B010184	B010196	CIRCUIT BD ASSY:MPU	80009	671-0058-04
A1	671-0058-06	B010197	B010223	CIRCUIT BD ASSY:MPU	80009	671-0058-06
A1	671-0058-07	B010224	B010224	CIRCUIT BD ASSY:MPU	80009	671-0058-07
A1	671-0058-09	B010225	B020114	CIRCUIT BD ASSY:MPU	80009	671-0058-09
A1	671-0058-10	B020115	B020184	CIRCUIT BD ASSY:MPU	80009	671-0058-10
A1	671-0058-11	B020185	B020299	CIRCUIT BD ASSY:MPU	80009	671-0058-11
A1	671-0058-12	B020300	B020303	CIRCUIT BD ASSY:MPU	80009	671-0058-12
A1	671-0058-13	B020304	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-13
A1	671-0058-14	B030100		CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	671-0058-14
A1	671-0058-03	B010100	B010173	CIRCUIT BD ASSY:MPU	80009	671-0058-03
A1	671-0058-04	B010174	B010220	CIRCUIT BD ASSY:MPU	80009	671-0058-04
A1	671-0058-05	B010221	B010224	CIRCUIT BD ASSY:MPU	80009	671-0058-05
A1	671-0058-06	B010225	B010255	CIRCUIT BD ASSY:MPU	80009	671-0058-06
A1	671-0058-07	B010256	B010345	CIRCUIT BD ASSY:MPU	80009	671-0058-07
A1	671-0058-08	B010346	B010475	CIRCUIT BD ASSY:MPU	80009	671-0058-08
A1	671-0058-09	B010476	B010794	CIRCUIT BD ASSY:MPU	80009	671-0058-09
A1	671-0058-10	B010795	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-10
A1	671-0058-11	B030100	B050276	CIRCUIT BD ASSY:MPU	80009	671-0058-11
A1	671-0058-12	B050277	B060164	CIRCUIT BD ASSY:MPU	80009	671-0058-12
A1	671-0058-13	B060165	B069999	CIRCUIT BD ASSY:MPU	80009	671-0058-13
A1	671-0058-14	B070100		CIRCUIT BD ASSY:MPU (3002 ONLY)	80009	671-0058-14
A1A1	671-0058-00	B010100	B010154	CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	671-0058-00
A1A2	671-0980-00	B010100	B010154	CIRCUIT BD ASSY:VIDEO FILTER (2510 ONLY)	80009	671-0980-00
A14	671-0058-51	B010100	B010113	CIRCUIT BD ASSY:MPU	80009	671-0058-51
A14	671-0058-52	B010114	B010125	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010126	B010128	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010129		CIRCUIT BD ASSY:MPU (3001MPM ONLY)	80009	671-0058-54
A14	671-0058-52	B010100	B010140	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010141	B010159	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010160	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B030100	B039999	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B040100	B049999	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B050100	B059999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B060100		CIRCUIT BD ASSY:MPU (3001HSM ONLY)	80009	671-0058-58
A14	671-0058-51	B010100	B010174	CIRCUIT BD ASSY:MPU	80009	671-0058-51
A14	671-0058-52	B010175	B010190	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010191	B010209	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010210	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B020100	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B030100	B040104	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B040105	B049999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B050100		CIRCUIT BD ASSY:MPU (3001MPX ONLY)	80009	671-0058-58
A14	671-0058-56	B010100	B010169	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B010170	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B020100		CIRCUIT BD ASSY:MPU (3001GPX ONLY)	80009	671-0058-58

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14	671-0058-54	B010100	B010248	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B010249	B010281	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B010282	B010287	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B010288	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B020100		CIRCUIT BD ASSY:MPU (2505 ONLY)	80009	671-0058-58

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1	672-1304-00	B010100	B010154	CIRCUIT BD ASSY:MPU	80009	672-1304-00
A1	671-0058-01	B010155	B010164	CIRCUIT BD ASSY:MPU	80009	671-0058-01
A1	671-0058-02	B010165	B010166	CIRCUIT BD ASSY:MPU	80009	671-0058-02
A1	671-0058-03	B010167	B010183	CIRCUIT BD ASSY:MPU	80009	671-0058-03
A1	671-0058-04	B010184	B010196	CIRCUIT BD ASSY:MPU	80009	671-0058-04
A1	671-0058-06	B010197	B010223	CIRCUIT BD ASSY:MPU	80009	671-0058-06
A1	671-0058-07	B010224	B010224	CIRCUIT BD ASSY:MPU	80009	671-0058-07
A1	671-0058-09	B010225	B020114	CIRCUIT BD ASSY:MPU	80009	671-0058-09
A1	671-0058-10	B020115	B020184	CIRCUIT BD ASSY:MPU	80009	671-0058-10
A1	671-0058-11	B020185	B020299	CIRCUIT BD ASSY:MPU	80009	671-0058-11
A1	671-0058-12	B020300	B020303	CIRCUIT BD ASSY:MPU	80009	671-0058-12
A1	671-0058-13	B020304	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-13
A1	671-0058-14	B030100		CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	671-0058-14
A1	671-0058-03	B010100	B010173	CIRCUIT BD ASSY:MPU	80009	671-0058-03
A1	671-0058-04	B010174	B010220	CIRCUIT BD ASSY:MPU	80009	671-0058-04
A1	671-0058-05	B010221	B010224	CIRCUIT BD ASSY:MPU	80009	671-0058-05
A1	671-0058-06	B010225	B010255	CIRCUIT BD ASSY:MPU	80009	671-0058-06
A1	671-0058-07	B010256	B010345	CIRCUIT BD ASSY:MPU	80009	671-0058-07
A1	671-0058-08	B010346	B010475	CIRCUIT BD ASSY:MPU	80009	671-0058-08
A1	671-0058-09	B010476	B010794	CIRCUIT BD ASSY:MPU	80009	671-0058-09
A1	671-0058-10	B010795	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-10
A1	671-0058-11	B030100	B050276	CIRCUIT BD ASSY:MPU	80009	671-0058-11
A1	671-0058-12	B050277	B060164	CIRCUIT BD ASSY:MPU	80009	671-0058-12
A1	671-0058-13	B060165	B069999	CIRCUIT BD ASSY:MPU	80009	671-0058-13
A1	671-0058-14	B070100		CIRCUIT BD ASSY:MPU (3002 ONLY)	80009	671-0058-14
A1BT275	146-0063-00			BATTERY,DRY:3V,150MAH,BUTTON CELL	61058	BR2325
A1C104	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C105	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C110	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C201	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C203	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C205	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C210	290-0527-00			CAP,FXD,ELCTLT:15UF,20%,20V	31433	T355F156M020AS
A1C211	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C215	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C216	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C216	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C219	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C219	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C221	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C221	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C226	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C226	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C229	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C229	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA

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A1C231	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C231	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C235	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C236	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C236	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C238	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C238	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C239	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C239	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C248	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C249	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C250	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C255	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C290	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	SA101C103KAA
A1C310	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C313	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C318	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C320	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C325	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C325	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C328	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C328	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C330	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C330	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C331	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C331	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C335	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C335	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C336	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C336	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C338	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C338	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C339	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C339	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA

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A1C340	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C340	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C341	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C341	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C345	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C345	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C348	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C348	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C370	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C375	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C380	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C385	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C386	281-0913-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C386	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C400	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C415	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C418	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C420	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C427	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C428	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C429	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C430	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C435	281-0913-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C435	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C436	281-0814-00	B010174	B029999	CAP,FXD,CER DI:100 PF,10%,100V (3002 ONLY)	04222	SA102A101KAA
A1C436	281-0814-00	B010184	B020184	CAP,FXD,CER DI:100 PF,10%,100V (2510 ONLY)	04222	SA102A101KAA
A1C437	281-0909-00	B010100	B020184	CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C437	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C440	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C441	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A1C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C450	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C455	281-0219-00	B010100	B020184	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A1C455	281-0797-00	B020185		CAP,FXD,CER DI:15PF,10%,100V (2510 ONLY)	04222	SA102A150KAA
A1C455	281-0219-00	B010100	B029999	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A1C455	281-0797-00	B030100		CAP,FXD,CER DI:15PF,10%,100V (3002 ONLY)	04222	SA102A150KAA

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A1C458	283-0186-00	B010100	B020184	CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A1C458	281-0797-00	B020185		CAP,FXD,CER DI:15PF,10%,100V (2510 ONLY)	04222	SA102A150KAA
A1C458	283-0186-00	B010100	B029999	CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A1C458	281-0797-00	B030100		CAP,FXD,CER DI:15PF,10%,100V (3002 ONLY)	04222	SA102A150KAA
A1C459	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C475	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C480	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C480	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C485	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C500	290-0531-00			CAP,FXD,ELCTLT:100UF,20%,10V	31433	T354J107M010AS
A1C504	283-0198-00			CAP,FXD,CER DI:0.22UF,20%,50V	04222	SR305C224MAA
A1C506	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	31433	T322B105M035AS
A1C508	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C509	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C510	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C511	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C514	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C515	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C516	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C517	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C525	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C528	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C535	281-0913-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C535	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C536	281-0814-00	B010174	B029999	CAP,FXD,CER DI:100 PF,10%,100V	04222	SA102A101KAA
A1C536	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C536	281-0814-00	B010184	B020184	CAP,FXD,CER DI:100 PF,10%,100V	04222	SA102A101KAA
A1C536	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C538	281-0909-00	B020185		CAP,FXD,CER DI:0.022UF,20%,50V (2510 ONLY)	04222	SA105C223MAA
A1C538	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3002 ONLY)	04222	SA105C223MAA
A1C540	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C548	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C559	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C600	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C601	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	SA102A100KAA
A1C611	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C635	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C648	281-0913-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C648	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C655	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1C660	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C700	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

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A1C704	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1C705	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C707	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C708	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C710	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C711	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C712	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C713	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C715	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C718	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C719	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C724	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C725	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C730	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C735	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C738	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C748	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C750	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C752	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C758	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA
A1C759	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C759	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C760	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C800	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1C804	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1C805	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1C807	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA
A1C810	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1C811	281-0759-00	B010100	B020184	CAP,FXD,CER DI:22PF,10%,100V (2510 ONLY)	04222	SA102A220KAA
A1C811	281-0759-00	B010100	B029999	CAP,FXD,CER DI:22PF,10%,100V (3002 ONLY)	04222	SA102A220KAA
A1C813	281-0775-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,20%,50V (2510 ONLY)	04222	SA105E104MAA
A1C813	281-0775-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,20%,50V (3002 ONLY)	04222	SA105E104MAA
A1C814	281-0775-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C814	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C814	281-0775-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C814	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C816	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C816	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA
A1C817	281-0786-00	B010100	B020184	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C817	281-0913-00	B020185		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2510 ONLY)	04222	SA105E104ZAA
A1C817	281-0786-00	B010100	B029999	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C817	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3002 ONLY)	04222	SA105E104ZAA

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A1C818	281-0913-00	B010100	B020184	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C818	281-0759-00	B020185		CAP,FXD,CER DI:22PF,10%,100V (2510 ONLY)	04222	SA102A220KAA
A1C818	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C818	281-0759-00	B030100		CAP,FXD,CER DI:22PF,10%,100V (3002 ONLY)	04222	SA102A220KAA
A1C819	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C820	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C821	281-0786-00	B020185		CAP,FXD,CER DI:150PF,10%,100V (2510 ONLY)	04222	SA101A151KAA
A1C821	281-0786-00	B030100		CAP,FXD,CER DI:150PF,10%,100V (3002 ONLY)	04222	SA101A151KAA
A1C825	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C830	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C831	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C832	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C833	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C834	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C835	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C836	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1C838	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C848	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C857	281-0814-01			CAP,FXD,CER DI:100PF,5%,100V	04222	SA102A101JAA
A1CR750	152-0141-02			DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF	27014	FDH9427
A1CR855	152-0323-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	12954	MT5282
A1DL341	119-1446-00	B020185		DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG (2510 ONLY)	20933	00T167
A1DL341	119-1446-00	B030100		DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG (3002 ONLY)	20933	00T167
A1DL355	119-1446-00			DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG	20933	00T167
A1DL560	119-0500-00			DELAY LINE,ELEC:20NS	01961	PE 20411
A1DS490	150-1137-00			LAMP,INCAND:10 ELEMENT ARRAY	50434	HDSP-4836
A1F110	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F240	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A1F250	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F255	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A1F286	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F470	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F471	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F575	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A1F700	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A1F701	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A1F702	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A1F703	159-0152-00			FUSE,WIRE LEAD:5A,125V,FAST BLOW	61857	SP5-5A
A1J100	----- -----			CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.2 CTR (SEE FIG 1-8 RMPL)	TK1471	1748222
A1J105	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 2, SEE FIG 1-7 RMPL)	22526	48283-036
A1J110	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 5, SEE FIG 1-7 RMPL)	22526	48283-036
A1J115	----- -----			CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.156 (SEE FIG 1-6 RMPL)	27264	26-48-2056
A1J120	----- -----			CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (SEE FIG 1-5 RMPL)	22526	65496-025

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A1J140	----- -----			CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (SEE FIG 1-4 RMPL)	22526	65496-001
A1J150	----- -----			CONN,HDR PWR::PCB,;MALE,RTANG,1 X 4,0.2 CTR (SEE FIG 1-3 RMPL)	00779	641737-1
A1J160	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 5, SEE FIG 1-7 RMPL)	22526	48283-036
A1J170	----- -----			CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR (SEE FIG 1-2 RMPL)	22526	65496-019
A1J190	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 4, SEE FIG 1-7 RMPL)	22526	48283-036
A1J285	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 3, SEE FIG 1-7 RMPL)	22526	48283-036
A1J390	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 1, SEE FIG 1-7 RMPL)	22526	48283-036
A1J460	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 1, SEE FIG 1-7 RMPL)	22526	48283-036
A1J505	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 2, SEE FIG 1-7 RMPL)	22526	48283-036
A1J560	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 2, SEE FIG 1-7 RMPL)	22526	48283-036
A1J580	----- -----			CONN,RCPT,ELEC:SNAP,20 CONTACT (SEE FIG 1-19 RMPL)	00779	2-583900-8
A1J820	----- -----			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG (SEE FIG 1-40 RMPL)	53387	10226-52B2VE
A1J860	----- -----			CONN,RF JACK:PCB,PELTOLA;FEMALE,STR,0.141 (SEE FIG 1-26 RMPL)	80009	131-1003-00
A1J860	----- -----			SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H (SEE FIG 1-26A RMPL)	22526	75060-012
A1J870	----- -----			CONN,RCPT,ELEC:BNC,FEMALE (SEE FIG 1-33 RMPL)	24931	28JR364-1
A1J910	----- -----			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG (SEE FIG 1-40 RMPL)	53387	10226-52B2VE
A1J945	----- -----			SCREW LOCK:4-40 X 0.312 L HEX HD,STLCD PL (SEE FIG 1-39 RMPL)	0KB01	131-0890-00
A1J945	----- -----			CONN,DSUB:PCB,,;MALE,RTANG,25 POS,0.318 PCB (SEE FIG 1-38 RMPL)	00779	747842-4
A1J950	----- -----			CONN,RF JACK:BNC,;50 OHM,FEMALE,RTANG (SEE FIG 1-34 RMPL)	00779	227677-1
A1L510	108-0317-00			COIL,RF:FIXED,15 UH	0JR03	108-0317-00
A1L600	108-0182-00			COIL,RF:FIXED,293NH	0JR03	108-0182-00
A1L800	108-0864-00	B010100	B029999	COIL,RF:FIXED,71NH (3002 ONLY)	0JR03	108-0864-00
A1L800	108-0864-00	B010167	B020184	COIL,RF:FIXED,71NH (2510 ONLY)	0JR03	108-0864-00
A1L801	108-0864-00	B020185		COIL,RF:FIXED,71NH (2510 ONLY)	0JR03	108-0864-00
A1L801	108-0864-00	B030100		COIL,RF:FIXED,71NH (3002 ONLY)	0JR03	108-0864-00
A1L808	108-0733-00			COIL,RF:FIXED,117NH	0JR03	108-0733-00
A1L817	276-0818-00			COIL,EM:100MHZ,FERRITE,BEAD ON LEAD, IMP:	34899	2743003112
A1L818	108-0245-00			CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A1L860	108-0245-00			CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A1Q285	151-1121-00			TRANSISTOR,PWR:MOS,N-CH;60V,0.5A,3.0 OHM	59640	VN0106N3
A1Q402	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q403	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q404	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q800	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q850	151-1090-00			TRANSISTOR,SIG:JFET,N-CH;DUAL,5V,25MA,6.5MS	TK1864	SNJ3003

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A1R160	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A1R161	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R211	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R213	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R214	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R215	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R216	315-0512-00	B010197	B020184	RES,FXD,FILM:5.1K OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E05K1
A1R216	315-0512-00	B010225	B029999	RES,FXD,FILM:5.1K OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E05K1
A1R240	315-0300-00	B020185		RES,FXD,FILM:30 OHM,5%,0.25W (2510 ONLY)	19701	5043CX30R00J
A1R240	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3002 ONLY)	19701	5043CX30R00J
A1R241	315-0220-00	B020185		RES,FXD,FILM:22 OHM,5%,0.25W (2510 ONLY)	19701	5043CX22R00J
A1R241	315-0220-00	B030100		RES,FXD,FILM:22 OHM,5%,0.25W (3002 ONLY)	19701	5043CX22R00J
A1R242	315-0300-00	B020185		RES,FXD,FILM:30 OHM,5%,0.25W (2510 ONLY)	19701	5043CX30R00J
A1R242	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3002 ONLY)	19701	5043CX30R00J
A1R243	315-0220-00	B020185		RES,FXD,FILM:22 OHM,5%,0.25W (2510 ONLY)	19701	5043CX22R00J
A1R243	315-0220-00	B030100		RES,FXD,FILM:22 OHM,5%,0.25W (3002 ONLY)	19701	5043CX22R00J
A1R260	307-0503-00			RES NTWK,FXD,FI:(9) 510 OHM,20%	91637	MSP10A01-511G-D03
A1R285	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R286	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R310	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R311	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R324	315-0300-00	B020185		RES,FXD,FILM:30 OHM,5%,0.25W (2510 ONLY)	19701	5043CX30R00J
A1R324	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3002 ONLY)	19701	5043CX30R00J
A1R325	315-0512-00	B020185		RES,FXD,FILM:5.1K OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E05K1
A1R325	315-0512-00	B030100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E05K1
A1R326	315-0300-00	B020185		RES,FXD,FILM:30 OHM,5%,0.25W (2510 ONLY)	19701	5043CX30R00J
A1R326	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3002 ONLY)	19701	5043CX30R00J
A1R357	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R360	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R361	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R362	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R363	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R370	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	91637	CSC10B01-272J/G
A1R380	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A1R385	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A1R390	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R400	315-0102-00	B010197		RES,FXD,FILM:1K OHM,5%,0.25W (2510 ONLY)	57668	NTR25JE01K0
A1R400	315-0102-00	B010225		RES,FXD,FILM:1K OHM,5%,0.25W (3002 ONLY)	57668	NTR25JE01K0
A1R418	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R419	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1R438	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R458	315-0104-00	B010100	B020184	RES,FXD,FILM:100K OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E100K
A1R458	315-0104-00	B010100	B029999	RES,FXD,FILM:100K OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E100K
A1R460	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	91637	CSC10B01-272J/G
A1R461	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R465	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R470	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R475	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R483	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R490	307-0695-00			RES NTWK,FXD,FI:9,150 OHM,2%,0.2W EA	11236	750-101-R150 OHM OR
A1R500	311-1261-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A1R505	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A1R506	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1R507	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A1R508	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R510	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R511	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R513	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R514	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R516	315-0512-00	B020300		RES,FXD,FILM:5.1K OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E05K1
A1R516	315-0512-00	B050277		RES,FXD,FILM:5.1K OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E05K1
A1R518	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R600	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R605	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	91637	MSP06A01-1D1G OR CSC
A1R615	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R700	315-0511-00	B010100	B020184	RES,FXD,FILM:510 OHM,5%,0.25W (2510 ONLY)	19701	5043CX510R0J
A1R700	315-0511-00	B010100	B029999	RES,FXD,FILM:510 OHM,5%,0.25W (3002 ONLY)	19701	5043CX510R0J
A1R704	315-0103-00	B010100	B020184	RES,FXD,FILM:10K OHM,5%,0.25W (2510 ONLY)	19701	5043CX10K00J
A1R704	315-0103-00	B010100	B029999	RES,FXD,FILM:10K OHM,5%,0.25W (3002 ONLY)	19701	5043CX10K00J
A1R707	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R708	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R709	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	91637	MSP06A01-1D1G OR CSC
A1R710	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R712	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R713	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R714	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W (3002 ONLY)	91637	MSP06A01-1D1G OR CSC
A1R714	307-0526-00	B010155	B010166	RES NTWK,FXD,FI:5,510 OHM,10%,0.125W	91637	CSC06A01-511J-D03
A1R714	307-0488-00	B010167		RES NTWK,FXD,FI:5 100 OHM,20%,0.75W (2510 ONLY)	91637	MSP06A01-1D1G OR CSC
A1R715	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R720	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R745	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R750	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R751	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R752	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R753	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A1R755	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R756	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R757	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1R758	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A1R759	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A1R800	317-0120-00	B010100	B029999	RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A1R800	315-0120-00	B030100		RES,FXD,FILM:12 OHM,5%,0.25W (3002 ONLY)	19701	SFR25 2322-181-63120
A1R800	315-0620-00	B010155	B010166	RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R800	317-0120-00	B010167	B020184	RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A1R800	315-0120-00	B020185		RES,FXD,FILM:12 OHM,5%,0.25W (2510 ONLY)	19701	SFR25 2322-181-63120
A1R801	315-0221-00	B010100	B020184	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R801	315-0511-00	B020185		RES,FXD,FILM:510 OHM,5%,0.25W (2510 ONLY)	19701	5043CX510R0J
A1R801	315-0221-00	B010100	B029999	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R801	315-0511-00	B030100		RES,FXD,FILM:510 OHM,5%,0.25W (3002 ONLY)	19701	5043CX510R0J
A1R802	315-0101-00	B010100	B029999	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R802	315-0221-00	B030100		RES,FXD,FILM:220 OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E220E
A1R802	315-0511-00	B010155	B010166	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R802	315-0101-00	B010167	B020184	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R802	315-0221-00	B020185		RES,FXD,FILM:220 OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E220E
A1R803	315-0470-00	B010100	B020184	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R803	315-0101-00	B020185		RES,FXD,FILM:100 OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E 100E
A1R803	315-0470-00	B010100	B029999	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R803	315-0101-00	B030100		RES,FXD,FILM:100 OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E 100E
A1R804	315-0470-00	B020185		RES,FXD,FILM:47 OHM,5%,0.25W (2510 ONLY)	57668	NTR25J-E47E0
A1R804	315-0470-00	B030100		RES,FXD,FILM:47 OHM,5%,0.25W (3002 ONLY)	57668	NTR25J-E47E0
A1R805	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R806	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R807	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R813	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R815	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R816	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R817	315-0161-00			RES,FXD,FILM:160 OHM,5%,0.25W (3002 ONLY)	19701	5043CX160R0J
A1R817	315-0102-00	B010155	B010166	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R817	315-0161-00	B010167		RES,FXD,FILM:160 OHM,5%,0.25W (2510 ONLY)	19701	5043CX160R0J
A1R818	315-0103-00	B020185		RES,FXD,FILM:10K OHM,5%,0.25W (2510 ONLY)	19701	5043CX10K00J
A1R818	315-0103-00	B030100		RES,FXD,FILM:10K OHM,5%,0.25W (3002 ONLY)	19701	5043CX10K00J
A1R825	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCO
A1R826	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCO
A1R827	307-0598-00			RES NTWK,FXD,FI:7,330 OHM,2%,1.0WTC=250	91637	MSP08A01331G OR CSCO
A1R835	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCO
A1R836	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCO
A1R850	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R855	321-0030-00			RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=TOMI	91637	CMF55116G20R00F
A1R856	321-0481-00			RES,FXD,FILM:1M OHM,1%,0.125W,TC=TOMI	91637	CMF55116G10003F
A1R857	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K

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A1TP325	----- -----	B020185		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2510 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP325	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3002 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP375	----- -----	B020185		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2510 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP375	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3002 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP605	----- -----	B020185		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2510 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP605	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3002 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP760	----- -----	B020185		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2510 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1TP760	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3002 ONLY, SEE FIG 1-7 RMPL)	22526	48283-036
A1U205	156-1381-00			IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY;THREE	34371	CA3096AE-17
A1U211	156-2396-00			IC,MISC:BIPOLAR,PWR SUPPLY SUPERVISOR;MPU	01295	TL7705 ACP
A1U213	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U215	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U215	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U216	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U216	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U218	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U218	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U219	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U219	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U220	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U220	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U221	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U221	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U225	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U225	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U226	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U226	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U228	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U228	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U229	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U229	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1U230	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U230	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U231	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U231	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U235	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U235	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U236	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U236	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U238	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U238	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U239	156-4030-00	B020185		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2510 ONLY)	0JR04	TC514400Z-10
A1U239	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3002 ONLY)	0JR04	TC514400Z-10
A1U248	156-0385-00	B010100	B010794	IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A1U248	156-0645-00	B010795		IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (3002 ONLY)	01295	SN74LS14N
A1U248	156-0385-00	B010100	B020114	IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A1U248	156-0645-00	B020115		IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (2510 ONLY)	01295	SN74LS14N
A1U250	156-2041-01			IC,PROCESSOR:NMOS,PERIPHERAL;FLOPPY DISK	66302	VL1772-02PC
A1U255	156-2184-00			IC,DIGITAL:HCTCMOS,BUFFER;INV OCTAL, LINE	01295	SN74HCT240N
A1U260	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U315	156-1726-00			IC,DIGITAL:FTTL,DEMUX/DECODER;DUAL 1-OF-4	04713	MC74F139 N
A1U318	156-1962-00			IC,DIGITAL:FTTL,BUFFER;OCTAL NONINV	04713	MC74F244N
A1U320	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A1U325	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U325	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U328	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U328	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U330	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U330	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U331	156-1722-00	B020185	B020303	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A1U331	156-0385-00	B020304		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (2510 ONLY)	01295	SN74LS04N
A1U331	156-1722-00	B030100	B060164	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A1U331	156-0385-00	B060165		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3002 ONLY)	01295	SN74LS04N
A1U335	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U335	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10

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A1U336	156-1722-00	B020185	B020303	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A1U336	156-0385-00	B020304		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (2510 ONLY)	01295	SN74LS04N
A1U336	156-1722-00	B030100	B060164	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A1U336	156-0385-00	B060165		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3002 ONLY)	01295	SN74LS04N
A1U338	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U338	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U339	160-8763-00	B020185		IC,DIGITAL:STTL,PLD;16L8,PRGM 156-1809-03 (2510 ONLY)	80009	156180903
A1U339	160-8763-00	B030100		IC,DIGITAL:STTL,PLD;16L8,PRGM 156-1809-03 (3002 ONLY)	80009	156180903
A1U340	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U340	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U345	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U345	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U348	156-2972-00	B010100	B020184	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2510 ONLY)	0JR04	TC511000AP-10
A1U348	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3002 ONLY)	0JR04	TC511000AP-10
A1U350	156-2478-00			IC,PROCESSOR:CMOS,PERIPHERAL;RTC, CLOCK	34371	ICM7170CPG/IPG
A1U360	156-1746-00			IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A1U365	156-0385-00			IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A1U370	156-0381-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT XOR	01295	SN74LS86AN
A1U375	156-0388-00			IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D W/SET &	01295	SN74LS74AN
A1U380	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U385	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A1U400	160-5952-00	B010100	B010224	MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A1U400	160-5952-01	B010225		MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM (3002 ONLY)	80009	160-5952-01
A1U400	160-5952-00	B010155	B010196	MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A1U400	160-5952-01	B010197		MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM (2510 ONLY)	80009	160-5952-01
A1U410	160-5085-01	B010100	B010173	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-01
A1U410	160-5085-02	B010174	B010475	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-02
A1U410	160-5085-03	B010476	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-03
A1U410	160-5085-04	B030100	B069999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5084-04
A1U410	160-5085-05	B070100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002 ONLY)	80009	160-5084-05
A1U410	160-5085-01	B010100	B010183	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-01
A1U410	160-5085-02	B010184	B010224	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-02
A1U410	160-5085-03	B010225	B020184	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-03
A1U410	160-5085-04	B020185	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-04
A1U410	160-5085-04	B030100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (2510 ONLY)	80009	160-5085-05
A1U415	160-5086-01	B010100	B010173	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-01
A1U415	160-5086-02	B010174	B010475	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-02
A1U415	160-5086-03	B010476	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-03
A1U415	160-5086-04	B030100	B069999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A1U415	160-5086-05	B070100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002 ONLY)	80009	160-5086-05

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1U415	160-5086-01	B010100	B010183	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-01
A1U415	160-5086-02	B010184	B010224	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-02
A1U415	160-5086-03	B010225	B020184	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-03
A1U415	160-5086-04	B020185	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A1U415	160-5086-05	B030100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (2510 ONLY)	80009	160-5086-05
A1U420	156-2610-01	B010100	B010173	IC,PROCESSOR:NMOS,MICROPROCESSOR;16-BIT	04713	MC68010-RC10
A1U420	156-2174-00	B010174		IC,PROCESSOR:NMOS,MICROPROCESSOR;16-BIT (3002 ONLY)	04713	MC68010RC12
A1U420	156-2610-01	B010155	B010183	IC,PROCESSOR:NMOS,MICROPROCESSOR;16-BIT	04713	MC68010-RC10
A1U420	156-2174-00	B010184		IC,PROCESSOR:NMOS,MICROPROCESSOR;16-BIT (2510 ONLY)	04713	MC68010RC12
A1U430	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U435	156-1740-00	B010100	B020184	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (2510 ONLY)	34335	AM2966PC
A1U435	156-1740-00	B010100	B029999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (3002 ONLY)	34335	AM2966PC
A1U438	156-0467-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NAND	01295	SN74LS38N
A1U440	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U465	156-0392-00			IC,DIGITAL:LSTTL,FLIP FLOP;QUAD D W/CLR	01295	SN74LS175N
A1U470	156-0383-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NOR	01295	SN74LS02N
A1U475	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U480	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A1U485	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1U500	156-2782-00			IC,LINEAR:BIPOLAR,VOLTAGE REGULATOR	27014	LM337H
A1U513	156-1373-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;QUAD,	01295	SN74LS125AN
A1U515	156-1998-00			IC,DIGITAL:ALSTTL,FLIP FLOP;OCTAL D-TYPE	01295	SN74ALS273N
A1U518	160-4089-00			MICROCKT,DGTL:CMOS,GLUE ARRAY,PRGM3.5K	61892	UPD65042S-326
A1U525	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U528	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U535	156-1740-00	B010100	B020184	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (2510 ONLY)	34335	AM2966PC
A1U535	156-1740-00	B010100	B029999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (3002 ONLY)	34335	AM2966PC
A1U536	156-3001-00	B020185		IC,DIGITAL:TTL,BUFFER/DRIVER;11-BIT DYNAMIC (2510 ONLY)	34335	AM2976PC
A1U536	156-3001-00	B030100		IC,DIGITAL:TTL,BUFFER/DRIVER;11-BIT DYNAMIC (3002 ONLY)	34335	AM2976PC
A1U538	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A1U545	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A1U550	156-1737-00			IC,PROCESSOR:MOS,PERIPHERAL;DUART,SCRN;2681	18324	SCN2681AC1 (N40 OR I
A1U555	156-1746-00			IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A1U558	156-0878-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A1U605	156-0631-00			IC,DIGITAL:ECL,GATE;QUAD 2-INPUT OR/NOR	04713	MC10101(L OR P)
A1U610	156-2142-00			IC,DIGITAL:ECL,COUNTER;4-BIT BINARY;10H016	04713	MC10H016(P OR L)
A1U635	156-0469-00			IC,DIGITAL:LSTTL,DEMUX/DECODER;3-TO-8	01295	SN74LS138 (N OR J)
A1U655	156-3053-00			IC,DIGITAL:ACMOS,GATE;QUAD 2-INPUT NAND	27014	74AC00PC
A1U660	156-0878-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A1U700	156-3349-00			IC,DIGITAL:ACMOS,FLIP FLOP;HEX D-TYPE,CLEAR	27014	74AC174PC
A1U705	156-2350-00			IC,DIGITAL:ECL,TRANSLATOR;QUAD ECL-TO-TTL	04713	MC10H350 P OR L
A1U708	156-3060-00			IC,DIGITAL:ACMOS,FLIP FLOP;DUAL D-TYPE	27014	74AC74PC
A1U710	156-1639-00			IC,DIGITAL:ECL,FLIP FLOP;DUAL MASTER-SLAVE	04713	MC10H131(P OR L)
A1U713	156-2540-00			IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT NAND	18324	N74F38 N OR F
A1U715	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A1U720	160-4091-00			MICROCKT,DGTL:CMOS,COMMUNICATION ARRAY,3.5K	61892	UPD65031S349
A1U730	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U735	156-1611-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE;74F74	04713	MC74F74N
A1U745	160-4090-00			MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM10K	61892	UPD65101S143

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A1U750	156-0879-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE DRIVER	04713	MC1488P
A1U753	156-1226-00			IC,LINEAR:BIPOLAR,COMPARATOR;DUAL,OPEN	64155	LM319N
A1U836	156-3110-00			IC,DIGITAL:HCMOS,BUFFER;NONINV OCTAL, LINE	27014	MM74HC244N
A1W312	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A1W465	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A1W810	----- -----	B010100	B010223	CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	1Y013	62908
A1W810	----- -----	B010224		CA ASSY,SP,ELEC:26,28 AWG,4.0 L,RIBBON (2510 ONLY, SEE FIG 1-11 RMPL)	1Y013	62908
A1W810	----- -----	B010100	B010345	CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	1Y013	62908
A1W810	----- -----	B010346		CA ASSY,SP,ELEC:26,28 AWG,4.0 L,RIBBON (3002 ONLY, SEE FIG 1-11 RMPL)	1Y013	62908
A1W860	----- -----			CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2 (SEE FIG 1-27 RMPL)	80009	175-6657-00
A1Y455	158-0305-00			XTAL UNIT,QTZ:32.768 MHZ,0.001%,CL=9PF	51791	FCX-1V
A1Y600	158-0106-00			XTAL UNIT,QTZ:100MHZ,+/-0.0025%	75378	HC42/U
A1YG190	119-1427-01			XDCR,AUDIO:1-4.2KHZ,30MA,6V	63791	QMB-06
A1YG610	119-1460-00	B010100	B010255	OSC,XTAL,CLOCK:40.0MHZ	23875	MTO-T1-S3-40MHZ
A1YG610	119-3765-00	B010256		OSCILATOR,RF:40.045MHZ (3002 ONLY)	61429	F1100H-40.045MHZ
A1YG610	119-1460-00	B010155	B010223	OSC,XTAL,CLOCK:40.0MHZ	23875	MTO-T1-S3-40MHZ
A1YG610	119-3765-00	B010224		OSCILATOR,RF:40.045MHZ (2510 ONLY)	61429	F1100H-40.045MHZ

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1A1	671-0058-00	B010100	B010154	CIRCUIT BD ASSY:M.P.U. (2510 ONLY)	80009	671-0058-00
A1A1BT275	146-0063-00	B010100	B010154	BATTERY,DRY:3V,150MAH,BUTTON CELL	61058	BR2325
A1A1C104	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C105	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C110	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C205	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C215	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C248	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C250	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C255	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C260	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C268	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C310	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C313	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C318	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C320	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C350	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C360	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C365	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C370	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C375	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C378	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C380	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C386	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C400	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C415	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C428	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C429	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C430	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C435	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C440	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C448	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C450	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C458	283-0159-00	B010100	B010154	CAP,FXD,CER DI:18PF,5%,50V	04222	SR155A180JAA
A1A1C459	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C468	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C470	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C508	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C509	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C510	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C511	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C514	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C515	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C516	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C517	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C525	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C528	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C535	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C540	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C548	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C559	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C600	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C601	281-0811-00	B010100	B010154	CAP,FXD,CER DI:10PF,10%,100V	04222	SA102A100KAA
A1A1C635	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

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A1A1C648	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C655	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1A1C660	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C700	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C705	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C707	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C708	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C710	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C711	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C713	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C715	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C718	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C719	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C724	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C725	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C730	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C735	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C738	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C748	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C750	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C752	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C758	290-0782-00	B010100	B010154	CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA
A1A1C760	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C804	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1A1C805	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1A1C810	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A1A1C813	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C815	283-0177-00	B010100	B010154	CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1A1C816	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C817	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C819	290-0782-00	B010100	B010154	CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA
A1A1C825	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C826	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C838	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C848	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C859	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C869	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1F240	159-0204-00	B010100	B010154	FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A1A1F255	159-0204-00	B010100	B010154	FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A1A1F702	159-0221-00	B010100	B010154	FUSE,WIRE LEAD:0.500A,125V,S20W	61857	SP5-500 MA
A1A1J105	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 2 EA)	22526	48283-036
A1A1J110	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 5 EA)	22526	48283-036
A1A1J115	131-4262-00	B010100	B010154	CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.156	27264	26-48-2056
A1A1J140	131-3976-00	B010100	B010154	CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR	22526	65496-001
A1A1J150	131-4037-00	B010100	B010154	CONN,HDR PWR::PCB,;MALE,RTANG,1 X 4,0.2 CTR	00779	641737-1
A1A1J160	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 5 EA)	22526	48283-036
A1A1J170	131-3975-00	B010100	B010154	CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR	22526	65496-019
A1A1J190	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 4 EA)	22526	48283-036
A1A1J285	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 3 EA)	22526	48283-036
A1A1J390	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 1 EA)	22526	48283-036

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A1A1J460	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 1 EA)	22526	48283-036
A1A1J505	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 2 EA)	22526	48283-036
A1A1J560	131-0608-00	B010100	B010154	TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QUANTITY OF 2 EA)	22526	48283-036
A1A1J580	131-3947-00	B010100	B010154	CONN,RCPT,ELEC:SNAP,20 CONTACT	00779	2-583900-8
A1A1J860	131-1003-00	B010100	B010154	CONN,RF JACK:PCB,PELTOLA;FEMALE,STR,0.141	80009	131-1003-00
A1A1J860	136-0252-07	B010100	B010154	SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H	22526	75060-012
A1A1J870	131-1171-00	B010100	B010154	CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR364-1
A1A1J910	131-4495-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	10226-52B2VE
A1A1L510	108-0317-00	B010100	B010154	COIL,RF:FIXED,15 UH	0JR03	108-0317-00
A1A1L600	108-0182-00	B010100	B010154	COIL,RF:FIXED,293NH	0JR03	108-0182-00
A1A1L815	108-0245-00	B010100	B010154	CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A1A1L860	108-0245-00	B010100	B010154	CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A1A1Q503	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1A1Q510	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1A1Q511	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1A1Q850	151-1090-00	B010100	B010154	TRANSISTOR,SIG:JFET,N-CH;DUAL,5V,25MA,6.5MS	TK1864	SNJ3003
A1A1R211	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R212	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R213	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R215	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R260	307-0503-00	B010100	B010154	RES NTWK,FXD,FI:(9) 510 OHM,20%	91637	MSP10A01-511G-D03
A1A1R286	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R360	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R361	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R362	315-0471-00	B010100	B010154	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1A1R363	315-0471-00	B010100	B010154	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1A1R390	315-0151-00	B010100	B010154	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1A1R418	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R438	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R458	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R475	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R500	311-1261-00	B010100	B010154	RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A1A1R510	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R511	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R513	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R514	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R518	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R707	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1R708	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1R710	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R713	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R714	307-0526-00	B010100	B010154	RES NTWK,FXD,FI:5,510 OHM,10%,0.125 W	91637	CSC06A01-511J-D03
A1A1R715	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R720	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R745	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R750	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R751	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R752	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R755	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R756	315-0911-00	B010100	B010154	RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1A1R800	315-0620-00	B010100	B010154	RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1A1R802	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1R805	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1A1R806	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R807	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R815	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R816	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R817	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R820	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R821	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R822	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R823	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R855	321-0030-00	B010100	B010154	RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=TOMI	91637	CMF55116G20R00F
A1A1R856	321-0181-00	B010100	B010154	RES,FXD,FILM:750 OHM,1%,0.125W,TC=TO	91637	CMF55116G750R0F
A1A1R857	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R860	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1U211	156-2396-00	B010100	B010154	IC,MISC:BIPOLAR,PWR SUPPLY SUPERVISOR;MPU	01295	TL7705 ACP
A1A1U213	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U215	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U218	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U220	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U225	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U228	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U230	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U235	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U238	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U250	156-2041-01	B010100	B010154	IC,PROCESSOR:NMOS,PERIPHERAL;FLOPPY DISK	66302	VL1772-02PC
A1A1U260	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U315	156-1726-00	B010100	B010154	IC,DIGITAL:FTTL,DEMUX/DECODER;DUAL 1-OF-4	04713	MC74F139 N
A1A1U320	156-1111-00	B010100	B010154	IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV,	01295	SN74LS245N
A1A1U325	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U328	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U330	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U335	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U338	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U340	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U345	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U348	156-2972-00	B010100	B010154	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000	0JR04	TC511000AP-10
A1A1U360	156-1746-00	B010100	B010154	IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A1A1U370	156-0381-00	B010100	B010154	IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT XOR	01295	SN74LS86AN
A1A1U380	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U385	156-1111-00	B010100	B010154	IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV,	01295	SN74LS245N
A1A1U400	160-5952-00	B010100	B010154	MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A1A1U415	160-5086-00	B010100	B010154	MICROCKT,DGTL:NMOS,32768 X 8 EPROM.PRGM	80009	160-5086-00
A1A1U430	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U438	156-0467-00	B010100	B010154	IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NAND	01295	SN74LS38N
A1A1U470	156-0383-00	B010100	B010154	IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NOR	01295	SN74LS02N
A1A1U475	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U480	156-1111-00	B010100	B010154	IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV,	01295	SN74LS245N
A1A1U485	156-0956-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A1A1U513	156-1373-00	B010100	B010154	IC,DIGITAL:LSTTL,BUFFER/DRIVER;QUAD,	01295	SN74LS125AN
A1A1U538	156-2641-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A1A1U545	156-2641-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A1A1U550	156-1737-00	B010100	B010154	IC,PROCESSOR:MOS,PERIPHERAL;DUART,SCRN;2681	18324	SCN2681AC1 N40 OR I40
A1A1U555	156-1746-00	B010100	B010154	IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A1A1U558	156-0878-00	B010100	B010154	IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A1A1U655	156-3053-00	B010100	B010154	IC,DIGITAL:ACMOS,GATE;QUAD 2-INPUT NAND	27014	74AC00PC
A1A1U660	156-0878-00	B010100	B010154	IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A1A1U700	156-3349-00	B010100	B010154	IC,DIGITAL:ACMOS,FLIP FLOP;HEX D-TYPE,CLEAR	27014	74AC174PC

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1A1U713	156-2540-00	B010100	B010154	IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT NAND	18324	N74F38 N OR F
A1A1U715	156-1111-00	B010100	B010154	IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV,	01295	SN74LS245N
A1A1U720	160-4091-00	B010100	B010154	MICROCKT,DGTL:CMOS,COMMUNICATION ARRAY,3.5K	61892	UPD65031S349
A1A1U736	156-3110-00	B010100	B010154	IC,DIGITAL:HCMOS,BUFFER;NONINV OCTAL, LINE	27014	MM74HC244N
A1A1U745	160-4090-00	B010100	B010154	MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM10K	61892	UPD65101S143
A1A1W312	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A1A1W465	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A1A1W808	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A1A1W810	174-0595-00	B010100	B010154	CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	1Y013	62908
A1A1W860	175-6657-00	B010100	B010154	CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
A1A1YG610	119-1460-00	B010100	B010154	OSC,XTAL,CLOCK:40.0MHZ	23875	MTO-T1-S3-40MHZ

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1A2	671-0980-00	B010100	B010154	CIRCUIT BD ASSY:VIDEO FILTER (2510 ONLY)	80009	671-0980-00
A1A2C100	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A2C140	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A1A2J820	131-4495-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	10226-52B2VE
A1A2L100	276-0818-00	B010100	B010154	COIL,EM:100MHZ,FERRITE,BEAD ON LEAD, IMP:	34899	2743003112
A1A2R110	307-0598-00	B010100	B010154	RES NTWK,FXD,FI:7,330 OHM,2%,1.0WTC=250	91637	MSP08A01331G OR CSCO
A1A2R150	307-0677-00	B010100	B010154	RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCO
A1A2W153	175-0831-00	B010100	B010154	CABLE,SP,ELEC:8,26 AWG,STRD,PVC INSUL,RBN	08261	111-2699-971
A1A2W320	175-0828-00	B010100	B010154	CABLE,SP,ELEC:5,26 AWG,STRD,PVC JKT,RBN	08261	111-2699-955

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14	671-0058-51	B010100	B010113	CIRCUIT BD ASSY:MPU	80009	671-0058-51
A14	671-0058-52	B010114	B010125	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010126	B010128	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010129		CIRCUIT BD ASSY:MPU (3001MPM ONLY)	80009	671-0058-54
A14	671-0058-52	B010100	B010140	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010141	B010159	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010160	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B030100	B039999	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B040100	B049999	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B050100	B059999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B060100		CIRCUIT BD ASSY:MPU (3001HSM ONLY)	80009	671-0058-58
A14	671-0058-51	B010100	B010174	CIRCUIT BD ASSY:MPU	80009	671-0058-51
A14	671-0058-52	B010175	B010190	CIRCUIT BD ASSY:MPU	80009	671-0058-52
A14	671-0058-53	B010191	B010209	CIRCUIT BD ASST:MPU	80009	671-0058-53
A14	671-0058-54	B010210	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B020100	B029999	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B030100	B040104	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B040105	B049999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B050100		CIRCUIT BD ASSY:MPU (3001MPX ONLY)	80009	671-0058-58
A14	671-0058-56	B010100	B010169	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B010170	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B020100		CIRCUIT BD ASSY:MPU (3001GPX ONLY)	80009	671-0058-58
A14	671-0058-54	B010100	B010248	CIRCUIT BD ASSY:MPU	80009	671-0058-54
A14	671-0058-55	B010249	B010281	CIRCUIT BD ASSY:MPU	80009	671-0058-55
A14	671-0058-56	B010282	B010287	CIRCUIT BD ASSY:MPU	80009	671-0058-56
A14	671-0058-57	B010288	B019999	CIRCUIT BD ASSY:MPU	80009	671-0058-57
A14	671-0058-58	B020100		CIRCUIT BD ASSY:MPU (2505 ONLY)	80009	671-0058-58
A14BT275	146-0063-00			BATTERY,DRY:3V,150MAH,BUTTON CELL	61058	BR2325
A14C104	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C105	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C110	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C201	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C203	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C205	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C210	290-0527-00			CAP,FXD,ELCTLT:15UF,20%,20V	31433	T355F156M020AS
A14C211	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C215	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C216	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C216	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C216	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C219	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C219	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C219	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14C221	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C221	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C221	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C226	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C226	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C226	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C229	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C229	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C229	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C231	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C231	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C231	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C235	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C236	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C236	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C236	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C238	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C238	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C238	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C239	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C239	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C239	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C248	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C249	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C250	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C255	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C290	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	SA101C103KAA
A14C310	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C313	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C318	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C320	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14C325	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C325	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C325	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C328	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C328	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C328	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C330	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C330	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C330	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C331	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C331	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C331	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C335	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C335	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C335	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C336	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C336	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C336	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C338	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C338	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C338	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C339	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C339	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C339	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C340	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C340	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C340	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA

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A14C341	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C341	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C341	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C345	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C345	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C345	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C348	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C348	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C348	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C370	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C375	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C380	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C385	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C386	281-0913-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C386	281-0913-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C386	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C400	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C415	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C418	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C420	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C427	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C428	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C429	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C430	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C435	281-0913-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C435	281-0913-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C435	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C436	281-0814-00	B010100	B010248	CAP,FXD,CER DI:100 PF,10%,100V (2505 ONLY)	04222	SA102A101KAA
A14C436	281-0814-00	B010100	B019999	CAP,FXD,CER DI:100 PF,10%,100V (3001MPX ONLY)	04222	SA102A101KAA
A14C436	281-0814-00	B010100	B029999	CAP,FXD,CER DI:100 PF,10%,100V (3001HSM ONLY)	04222	SA102A101KAA
A14C437	281-0909-00	B010100	B010248	CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C437	281-0909-00	B010100	B019999	CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C437	281-0909-00	B010100	B029999	CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA

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A14C440	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C441	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	04222	SA105C223MAA
A14C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C450	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C455	281-0219-00	B010100	B010248	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A14C455	281-0797-00	B010249		CAP,FXD,CER DI:15PF,10%,100V (2505 ONLY)	04222	SA102A150KAA
A14C455	281-0219-00	B010100	B019999	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A14C455	281-0797-00	B020100		CAP,FXD,CER DI:15PF,10%,100V (3001MPX ONLY)	04222	SA102A150KAA
A14C455	281-0219-00	B010100	B029999	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A14C455	281-0797-00	B030100		CAP,FXD,CER DI:15PF,10%,100V (3001HSM ONLY)	04222	SA102A150KAA
A14C458	283-0186-00	B010100	B010248	CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A14C458	281-0797-00	B010249		CAP,FXD,CER DI:15PF,10%,100V (2505 ONLY)	04222	SA102A150KAA
A14C458	283-0186-00	B010100	B019999	CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A14C458	281-0797-00	B020100		CAP,FXD,CER DI:15PF,10%,100V (3001MPX ONLY)	04222	SA102A150KAA
A14C458	283-0186-00	B010100	B029999	CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A14C458	281-0797-00	B030100		CAP,FXD,CER DI:15PF,10%,100V (3001HSM ONLY)	04222	SA102A150KAA
A14C459	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C475	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C480	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C480	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C480	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C485	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C500	290-0531-00			CAP,FXD,ELCTLT:100UF,20%,10V	31433	T354J107M010AS
A14C504	283-0198-00			CAP,FXD,CER DI:0.22UF,20%,50V	04222	SR305C224MAA
A14C506	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	31433	T322B105M035AS
A14C508	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C509	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C510	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C511	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C514	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C515	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C516	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C517	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C525	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C528	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C535	281-0913-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C535	281-0913-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C535	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C536	281-0814-00	B010100	B010248	CAP,FXD,CER DI:100 PF,10%,100V	04222	SA102A101KAA
A14C536	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C536	281-0814-00	B010100	B019999	CAP,FXD,CER DI:100 PF,10%,100V	04222	SA102A101KAA
A14C536	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA

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A14C536	281-0814-00	B010100	B029999	CAP,FXD,CER DI:100 PF,10%,100V	04222	SA102A101KAA
A14C536	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C538	281-0909-00	B010249		CAP,FXD,CER DI:0.022UF,20%,50V (2505 ONLY)	04222	SA105C223MAA
A14C538	281-0909-00	B020100		CAP,FXD,CER DI:0.022UF,20%,50V (3001MPX ONLY)	04222	SA105C223MAA
A14C538	281-0909-00	B030100		CAP,FXD,CER DI:0.022UF,20%,50V (3001HSM ONLY)	04222	SA105C223MAA
A14C540	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C548	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C559	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C600	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C601	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	SA102A100KAA
A14C611	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C635	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C648	281-0913-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C648	281-0913-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C648	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C655	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A14C660	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C700	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C704	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A14C705	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C707	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C708	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C710	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C711	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C712	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C713	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C715	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C718	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C719	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C724	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C725	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C730	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C735	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C738	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C748	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C750	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C752	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C758	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA
A14C759	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C759	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C759	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C760	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C800	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A14C804	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A14C805	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A14C807	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	UVX1V4R7MAA

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A14C810	281-0268-00			CAP,FXD,CER DI:680PF,100V	04222	MA101A681KAA OR SA10
A14C811	281-0759-00	B010100	B010248	CAP,FXD,CER DI:22PF,10%,100V (2505 ONLY)	04222	SA102A220KAA
A14C811	281-0759-00	B010100	B019999	CAP,FXD,CER DI:22PF,10%,100V (3001MPX ONLY)	04222	SA102A220KAA
A14C811	281-0759-00	B010100	B029999	CAP,FXD,CER DI:22PF,10%,100V (3001HSM ONLY)	04222	SA102A220KAA
A14C813	281-0775-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,20%,50V (2505 ONLY)	04222	SA105E104MAA
A14C813	281-0775-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,20%,50V (3001MPX ONLY)	04222	SA105E104MAA
A14C813	281-0775-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,20%,50V (3001HSM ONLY)	04222	SA105E104MAA
A14C814	281-0775-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A14C814	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C814	281-0775-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A14C814	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C814	281-0775-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A14C814	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C816	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C816	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C816	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C817	281-0786-00	B010100	B010248	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C817	281-0913-00	B010249		CAP,FXD,CER DI:0.1UF,50V,AXIAL (2505 ONLY)	04222	SA105E104ZAA
A14C817	281-0786-00	B010100	B019999	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C817	281-0913-00	B020100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001MPX ONLY)	04222	SA105E104ZAA
A14C817	281-0786-00	B010100	B029999	CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C817	281-0913-00	B030100		CAP,FXD,CER DI:0.1UF,50V,AXIAL (3001HSM ONLY)	04222	SA105E104ZAA
A14C818	281-0913-00	B010100	B010248	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C818	281-0759-00	B010249		CAP,FXD,CER DI:22PF,10%,100V (2505 ONLY)	04222	SA102A220KAA
A14C818	281-0913-00	B010100	B019999	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C818	281-0759-00	B020100		CAP,FXD,CER DI:22PF,10%,100V (3001MPX ONLY)	04222	SA102A220KAA
A14C818	281-0913-00	B010100	B029999	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C818	281-0759-00	B030100		CAP,FXD,CER DI:22PF,10%,100V (3001HSM ONLY)	04222	SA102A220KAA
A14C819	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C820	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C821	281-0786-00	B010249		CAP,FXD,CER DI:150PF,10%,100V (2505 ONLY)	04222	SA101A151KAA
A14C821	281-0786-00	B020100		CAP,FXD,CER DI:150PF,10%,100V (3001MPX ONLY)	04222	SA101A151KAA
A14C821	281-0786-00	B030100		CAP,FXD,CER DI:150PF,10%,100V (3001HSM ONLY)	04222	SA101A151KAA
A14C825	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C826	283-0108-00	B010100	B010248	CAP,FXD,CER DI:220PF,10%,200V (2505 ONLY)	04222	SR152A221KAA
A14C826	283-0108-00	B010126		CAP,FXD,CER DI:220PF,10%,200V (3001MPM ONLY)	04222	SR152A221KAA

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A14C826	283-0108-00	B010141	B029999	CAP,FXD,CER DI:220PF,10%,200V (3001HSM ONLY)	04222	SR152A221KAA
A14C826	283-0108-00	B010191	B019999	CAP,FXD,CER DI:220PF,10%,200V (3001MPX ONLY)	04222	SR152A221KAA
A14C830	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C831	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C832	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C833	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C834	281-0786-00	B010100	B010125	CAP,FXD,CER DI:150PF,10%,100V (3001MPM ONLY)	04222	SA101A151KAA
A14C834	281-0786-00	B010100	B010140	CAP,FXD,CER DI:150PF,10%,100V (3001HSM ONLY)	04222	SA101A151KAA
A14C834	281-0786-00	B010100	B010190	CAP,FXD,CER DI:150PF,10%,100V (3001MPX ONLY)	04222	SA101A151KAA
A14C835	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C836	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	SA101A151KAA
A14C837	281-0863-00	B010249		CAP,FXD,CER DI:240PF,5%,100V (2505 ONLY)	04222	SA101A241JAA
A14C837	281-0863-00	B020100		CAP,FXD,CER DI:240PF,5%,100V (3001MPX ONLY)	04222	SA101A241JAA
A14C837	281-0863-00	B030100		CAP,FXD,CER DI:240PF,5%,100V (3001HSM ONLY)	04222	SA101A241JAA
A14C838	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C848	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C857	281-0814-01			CAP,FXD,CER DI:100PF,5%,100V	04222	SA102A101JAA
A14CR750	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A14CR855	152-0323-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	12954	MT5282
A14DL341	119-1446-00	B010249		DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG (2505 ONLY)	20933	00T167
A14DL341	119-1446-00	B020100		DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG (3001MPX ONLY)	20933	00T167
A14DL341	119-1446-00	B030100		DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG (3001HSM ONLY)	20933	00T167
A14DL355	119-1446-00			DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG	20933	00T167
A14DL560	119-0500-00			DELAY LINE,ELEC:20NS	01961	PE 20411
A14DS490	150-1137-00			LAMP,INCAND:10 ELEMENT ARRAY	50434	HDSP-4836
A14F110	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F240	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A14F250	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F255	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	61857	SP7-3A
A14F286	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F470	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F471	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F575	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	71400	MCR-1 1/2
A14F700	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A14F701	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A14F702	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A14F703	159-0152-00			FUSE,WIRE LEAD:5A,125V,FAST BLOW	61857	SP5-5A
A14J100	----- -----			CONN,HDR PWR::PCB,:MALE,RTANG,1 X 5,0.2 CTR (SEE FIG 2-8 RMPL)	TK1471	1748222
A14J105	----- -----			TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR,0.025 (QTY 2, SEE FIG 2-7 RMPL)	22526	48283-036
A14J110	----- -----			TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR,0.025 (QTY 5, SEE FIG 2-7 RMPL)	22526	48283-036
A14J115	----- -----			CONN,HDR PWR::PCB,:MALE,RTANG,1 X 5,0.156 (SEE FIG 2-6 RMPL)	27264	26-48-2056

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A14J120	----- -----			CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (2505 ONLY, SEE FIG 2-5 RMPL)	22526	65496-025
A14J120	----- -----	B010129		CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001MPM ONLY, SEE FIG 2-5 RMPL)	22526	65496-025
A14J120	----- -----	B010160		CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001HSM ONLY, SEE FIG 2-5 RMPL)	22526	65496-025
A14J120	----- -----	B010210		CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001MPX ONLY, SEE FIG 2-5 RMPL)	22526	65496-025
A14J140	----- -----			CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (2505 ONLY, SEE FIG 2-4 RMPL)	22526	65496-001
A14J140	----- -----	B010129		CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001MPM ONLY, SEE FIG 2-4 RMPL)	22526	65496-001
A14J140	----- -----	B010160		CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001HSM ONLY, SEE FIG 2-4 RMPL)	22526	65496-001
A14J140	----- -----	B010210		CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001MPX ONLY, SEE FIG 2-4 RMPL)	22526	65496-001
A14J150	----- -----			CONN,HDR PWR::PCB,;MALE,RTANG,1 X 4,0.2 CTR (SEE FIG 2-3 RMPL)	00779	641737-1
A14J160	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 5, SEE FIG 2-7 RMPL)	22526	48283-036
A14J170	----- -----			CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR (SEE FIG 2-2 RMPL)	22526	65496-019
A14J190	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 4, SEE FIG 2-7 RMPL)	22526	48283-036
A14J285	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 3, SEE FIG 2-7 RMPL)	22526	48283-036
A14J390	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 1, SEE FIG 2-7 RMPL)	22526	48283-036
A14J460	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 1, SEE FIG 2-7 RMPL)	22526	48283-036
A14J505	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 2, SEE FIG 2-7 RMPL)	22526	48283-036
A14J560	----- -----			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (QTY 2, SEE FIG 2-7 RMPL)	22526	48283-036
A14J580	----- -----			CONN,RCPT,ELEC:SNAP,20 CONTACT (SEE FIG 2-22 RMPL)	00779	2-583900-8
A14J810	131-4867-00	B010100	B010248	CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (2505 ONLY)	63058	ADP-63150-001
A14J810	131-4867-00	B010100	B019999	CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (3001MPX ONLY)	63058	ADP-63150-001
A14J810	131-4867-00	B010100	B029999	CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (3001HSM ONLY)	63058	ADP-63150-001
A14J820	131-4867-00	B010249		CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (2505 ONLY)	63058	ADP-63150-001
A14J820	131-4867-00	B020100		CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (3001MPX ONLY)	63058	ADP-63150-001
A14J820	131-4867-00	B030100		CONN,HDR::FEEDTHRU,;MALE,STR,35 POS,0.210 H (3001HSM ONLY)	63058	ADP-63150-001
A14J860	----- -----			CONN,RF JACK:PCB,PELTOLA;FEMALE,STR,0.141 (SEE FIG 2-26 RMPL)	80009	131-1003-00
A14J860	----- -----			SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H (SEE FIG 2-26A RMPL)	22526	75060-012
A14J870	----- -----			CONN,RCPT,ELEC:BNC,FEMALE (SEE FIG 2-33 RMPL)	24931	28JR364-1
A14J910	----- -----			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG (SEE FIG 2-40 RMPL)	53387	10226-52B2VE
A14J945	----- -----			SCREW LOCK:4-40 X 0.312 L HEX HD,STLCD PL (SEE FIG 2-39 RMPL)	0KB01	131-0890-00

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A14J945	----- -----			CONN,DSUB:PCB,,;MALE,RTANG,25 POS,0.318 PCB (SEE FIG 2-38 RMPL)	00779	747842-4
A14J950	----- -----			CONN,RF JACK:BNC,;50 OHM,FEMALE,RTANG (SEE FIG 2-34 RMPL)	00779	227677-1
A14L510	108-0317-00			COIL,RF:FIXED,15 UH	0JR03	108-0317-00
A14L600	108-0182-00			COIL,RF:FIXED,293NH	0JR03	108-0182-00
A14L800	108-0864-00	B010100	B010248	COIL,RF:FIXED,71NH (2505 ONLY)	0JR03	108-0864-00
A14L800	108-0864-00	B010100	B019999	COIL,RF:FIXED,71NH (3001MPX ONLY)	0JR03	108-0864-00
A14L800	108-0864-00	B010100	B029999	COIL,RF:FIXED,71NH (3001HSM ONLY)	0JR03	108-0864-00
A14L801	108-0864-00	B010249		COIL,RF:FIXED,71NH (2505 ONLY)	0JR03	108-0864-00
A14L801	108-0864-00	B020100		COIL,RF:FIXED,71NH (3001MPX ONLY)	0JR03	108-0864-00
A14L801	108-0864-00	B030100		COIL,RF:FIXED,71NH (3001HSM ONLY)	0JR03	108-0864-00
A14L808	108-0733-00			COIL,RF:FIXED,117NH	0JR03	108-0733-00
A14L817	276-0818-00			COIL,EM:100MHZ,FERRITE,BEAD ON LEAD, IMP:	34899	2743003112
A14L818	108-0245-00			CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A14L860	108-0245-00			CHOKE,RF:FIXED,3.9UH, +/- 10 %, Q 35, DCR	0JR03	108-0245-00
A140285	151-1121-00			TRANSISTOR,PWR:MOS,N-CH;60V,0.5A,3.0 OHM	59640	VN0106N3
A140402	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A140403	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A140404	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A140800	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A140850	151-1090-00			TRANSISTOR,SIG:JFET,N-CH;DUAL,5V,25MA,6.5MS	TK1864	SNJ3003
A14R160	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A14R161	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R211	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R213	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R214	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R215	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R216	315-0512-00	B010100	B010248	RES,FXD,FILM:5.1K OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E05K1
A14R216	315-0512-00	B010100	B019999	RES,FXD,FILM:5.1K OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E05K1
A14R216	315-0512-00	B010100	B029999	RES,FXD,FILM:5.1K OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E05K1
A14R240	315-0300-00	B010249		RES,FXD,FILM:30 OHM,5%,0.25W (2505 ONLY)	19701	5043CX30R00J
A14R240	315-0300-00	B020100		RES,FXD,FILM:30 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX30R00J
A14R240	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX30R00J
A14R241	315-0220-00	B010249		RES,FXD,FILM:22 OHM,5%,0.25W (2505 ONLY)	19701	5043CX22R00J
A14R241	315-0220-00	B020100		RES,FXD,FILM:22 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX22R00J
A14R241	315-0220-00	B030100		RES,FXD,FILM:22 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX22R00J
A14R242	315-0300-00	B010249		RES,FXD,FILM:30 OHM,5%,0.25W (2505 ONLY)	19701	5043CX30R00J
A14R242	315-0300-00	B020100		RES,FXD,FILM:30 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX30R00J
A14R242	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX30R00J

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A14R243	315-0220-00	B010249		RES,FXD,FILM:22 OHM,5%,0.25W (2505 ONLY)	19701	5043CX22R00J
A14R243	315-0220-00	B020100		RES,FXD,FILM:22 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX22R00J
A14R243	315-0220-00	B030100		RES,FXD,FILM:22 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX22R00J
A14R260	307-0503-00			RES NTWK,FXD,FI:(9) 510 OHM,20%	91637	MSP10A01-511G-D03
A14R285	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R286	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R310	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A14R311	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A14R324	315-0300-00	B010249		RES,FXD,FILM:30 OHM,5%,0.25W (2505 ONLY)	19701	5043CX30R00J
A14R324	315-0300-00	B020100		RES,FXD,FILM:30 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX30R00J
A14R324	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX30R00J
A14R325	315-0512-00	B010249		RES,FXD,FILM:5.1K OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E05K1
A14R325	315-0512-00	B020100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E05K1
A14R325	315-0512-00	B030100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E05K1
A14R326	315-0300-00	B010249		RES,FXD,FILM:30 OHM,5%,0.25W (2505 ONLY)	19701	5043CX30R00J
A14R326	315-0300-00	B020100		RES,FXD,FILM:30 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX30R00J
A14R326	315-0300-00	B030100		RES,FXD,FILM:30 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX30R00J
A14R357	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R360	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R361	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R362	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A14R363	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A14R370	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	91637	CSC10B01-272J/G
A14R380	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A14R385	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A14R390	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R400	315-0102-00	B010249		RES,FXD,FILM:1K OHM,5%,0.25W (2505 ONLY)	57668	NTR25JE01K0
A14R400	315-0102-00	B020100		RES,FXD,FILM:1K OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25JE01K0
A14R400	315-0102-00	B030100		RES,FXD,FILM:1K OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25JE01K0
A14R418	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R419	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A14R438	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R458	315-0104-00	B010100	B010248	RES,FXD,FILM:100K OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E100K
A14R458	315-0104-00	B010100	B019999	RES,FXD,FILM:100K OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E100K
A14R458	315-0104-00	B010100	B029999	RES,FXD,FILM:100K OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E100K
A14R460	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	91637	CSC10B01-272J/G
A14R461	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R465	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14R470	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R475	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R483	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R490	307-0695-00			RES NTWK,FXD,FI:9,150 OHM,2%,0.2W EA	11236	750-101-R150 OHM OR
A14R500	311-1261-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A14R505	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A14R506	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A14R507	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A14R508	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R510	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R511	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R513	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R514	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R516	315-0512-00	B040100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E05K1
A14R516	315-0512-00	B030100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E05K1
A14R516	315-0512-00	B010100		RES,FXD,FILM:5.1K OHM,5%,0.25W (3001GPX ONLY)	57668	NTR25J-E05K1
A14R516	315-0512-00	B010282		RES,FXD,FILM:5.1K OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E05K1
A14R518	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R600	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R605	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	91637	MSP06A01-1D1G OR CSC
A14R615	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R700	315-0511-00	B010100	B010248	RES,FXD,FILM:510 OHM,5%,0.25W (2505 ONLY)	19701	5043CX510R0J
A14R700	315-0511-00	B010100	B019999	RES,FXD,FILM:510 OHM,5%,0.25W (3001MPX)	19701	5043CX510R0J
A14R700	315-0511-00	B010100	B029999	RES,FXD,FILM:510 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX510R0J
A14R704	315-0103-00	B010100	B010248	RES,FXD,FILM:10K OHM,5%,0.25W (2505 ONLY)	19701	5043CX10K00J
A14R704	315-0103-00	B010100	B019999	RES,FXD,FILM:10K OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX10K00J
A14R704	315-0103-00	B010100	B029999	RES,FXD,FILM:10K OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX10K00J
A14R707	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R708	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R709	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	91637	MSP06A01-1D1G OR CSC
A14R710	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R712	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R713	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R714	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	91637	MSP06A01-1D1G OR CSC
A14R715	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R720	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R745	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R750	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R751	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A14R752	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R753	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A14R755	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R756	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A14R757	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A14R758	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A14R759	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14R800	317-0120-00	B010100	B010248	RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A14R800	315-0120-00	B010249		RES,FXD,FILM:12 OHM,5%,0.25W (2505 ONLY)	19701	SFR25 2322-181-63120
A14R800	317-0120-00	B010100	B019999	RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A14R800	315-0120-00	B020100		RES,FXD,FILM:12 OHM,5%,0.25W (3001MPX ONLY)	19701	SFR25 2322-181-63120
A14R800	317-0120-00	B010100	B029999	RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A14R800	315-0120-00	B030100		RES,FXD,FILM:12 OHM,5%,0.25W (3001HSM ONLY)	19701	SFR25 2322-181-63120
A14R801	315-0221-00	B010100	B010248	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A14R801	315-0511-00	B010249		RES,FXD,FILM:510 OHM,5%,0.25W (2505 ONLY)	19701	5043CX510R0J
A14R801	315-0221-00	B010100	B019999	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A14R801	315-0511-00	B020100		RES,FXD,FILM:510 OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX510R0J
A14R801	315-0221-00	B010100	B029999	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A14R801	315-0511-00	B030100		RES,FXD,FILM:510 OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX510R0J
A14R802	315-0101-00	B010100	B010248	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R802	315-0221-00	B010249		RES,FXD,FILM:220 OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E220E
A14R802	315-0101-00	B010100	B019999	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R802	315-0221-00	B020100		RES,FXD,FILM:220 OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E220E
A14R802	315-0101-00	B010100	B029999	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R802	315-0221-00	B030100		RES,FXD,FILM:220 OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E220E
A14R803	315-0470-00	B010100	B010248	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A14R803	315-0101-00	B010249		RES,FXD,FILM:100 OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E 100E
A14R803	315-0470-00	B010100	B019999	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A14R803	315-0101-00	B020100		RES,FXD,FILM:100 OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E 100E
A14R803	315-0470-00	B010100	B029999	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A14R803	315-0101-00	B030100		RES,FXD,FILM:100 OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E 100E
A14R804	315-0470-00	B010249		RES,FXD,FILM:47 OHM,5%,0.25W (2505 ONLY)	57668	NTR25J-E47E0
A14R804	315-0470-00	B020100		RES,FXD,FILM:47 OHM,5%,0.25W (3001MPX ONLY)	57668	NTR25J-E47E0
A14R804	315-0470-00	B030100		RES,FXD,FILM:47 OHM,5%,0.25W (3001HSM ONLY)	57668	NTR25J-E47E0
A14R805	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R806	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R807	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R813	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R815	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R816	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R817	315-0161-00			RES,FXD,FILM:160 OHM,5%,0.25W	19701	5043CX160R0J
A14R818	315-0103-00	B010249		RES,FXD,FILM:10K OHM,5%,0.25W (2505 ONLY)	19701	5043CX10K00J
A14R818	315-0103-00	B020100		RES,FXD,FILM:10K OHM,5%,0.25W (3001MPX ONLY)	19701	5043CX10K00J
A14R818	315-0103-00	B030100		RES,FXD,FILM:10K OHM,5%,0.25W (3001HSM ONLY)	19701	5043CX10K00J
A14R825	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCD
A14R826	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCD
A14R827	307-0598-00			RES NTWK,FXD,FI:7,330 OHM,2%,1.0WTC=250	91637	MSP08A01331G OR CSCD
A14R835	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCD
A14R836	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	91637	MSP08A03560G OR CSCD

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14R850	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A14R855	321-0030-00			RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=TOMI	91637	CMF55116G20R00F
A14R856	321-0481-00			RES,FXD,FILM:1M OHM,1%,0.125W,TC=TOMI	91637	CMF55116G10003F
A14R857	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A14TP325	----- -----	B010249		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2505 ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP325	----- -----	B020100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001MPX ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP325	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001HSM ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP375	----- -----	B010249		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2505 ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP375	----- -----	B020100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001MPX ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP375	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001HSM ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP605	----- -----	B010249		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2505 ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP605	----- -----	B020100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001MPX ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP605	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001HSM ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP760	----- -----	B010249		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (2505 ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP760	----- -----	B020100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001MPX ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14TP760	----- -----	B030100		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 (3001HSM ONLY, SEE FIG 2-7 RMPL)	22526	48283-036
A14U205	156-1381-00			IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY;THREE	34371	CA3096AE-17
A14U211	156-2396-00			IC,MISC:BIPOLAR,PWR SUPPLY SUPERVISOR;MPU	01295	TL7705 ACP
A14U213	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U215	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U215	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U215	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U216	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U216	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U216	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U218	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U218	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U218	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U219	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U219	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U219	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10

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A14U220	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U220	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U220	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U221	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U221	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U221	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U225	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U225	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U225	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U226	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U226	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U226	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U228	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U228	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U228	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U229	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U229	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U229	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U230	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U230	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U230	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U231	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U231	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U231	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U235	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U235	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U235	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10

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A14U236	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U236	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U236	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U238	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U238	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U238	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U239	156-4030-00	B010249		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (2505 ONLY)	0JR04	TC514400Z-10
A14U239	156-4030-00	B020100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001MPX ONLY)	0JR04	TC514400Z-10
A14U239	156-4030-00	B030100		IC,MEMORY:CMOS,DRAM;1 MEG X 4,FAST PAGE (3001HSM ONLY)	0JR04	TC514400Z-10
A14U248	156-0645-00			IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (2505 ONLY)	01295	SN74LS14N
A14U248	156-0385-00	B010100	B010128	IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A14U248	156-0645-00	B010129		IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (3001MPM ONLY)	01295	SN74LS14N
A14U248	156-0385-00	B010100	B010159	IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A14U248	156-0645-00	B010160		IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (3001HSM ONLY)	01295	SN74LS14N
A14U248	156-0385-00	B010100	B010209	IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A14U248	156-0645-00	B010210		IC,DIGITAL:LSTTL,GATES;HEX INV, W/SCHMITT (3001MPX ONLY)	01295	SN74LS14N
A14U250	156-2041-01			IC,PROCESSOR:NMOS,PERIPHERAL;FLOPPY DISK	66302	VL1772-02PC
A14U255	156-2184-00			IC,DIGITAL:HCTCMOS,BUFFER;INV OCTAL, LINE	01295	SN74HCT240N
A14U260	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U315	156-1726-00			IC,DIGITAL:FTTL,DEMUX/DECODER;DUAL 1-OF-4	04713	MC74F139 N
A14U318	156-1962-00			IC,DIGITAL:FTTL,BUFFER;OCTAL NONINV	04713	MC74F244N
A14U320	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A14U325	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U325	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U325	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U328	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U328	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U328	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U330	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U330	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U330	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14U331	156-1722-00	B010249	B010287	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U331	156-0385-00	B010288		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (2505 ONLY)	01295	SN74LS04N
A14U331	156-1722-00	B020100	B040104	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U331	156-0385-00	B040105		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001MPX ONLY)	01295	SN74LS04N
A14U331	156-1722-00	B030100	B049999	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U331	156-0385-00	B050100		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001HSM ONLY)	01295	SN74LS04N
A14U331	156-1722-00	B010100	B010169	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U331	156-0385-00	B010170		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001GPX ONLY)	01295	SN74LS04N
A14U335	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U335	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U335	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U336	156-1722-00	B010249	B010287	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U336	156-0385-00	B010288		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (2505 ONLY)	01295	SN74LS04N
A14U336	156-1722-00	B020100	B040104	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U336	156-0385-00	B040105		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001MPX ONLY)	01295	SN74LS04N
A14U336	156-1722-00	B030100	B049999	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U336	156-0385-00	B050100		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001HSM ONLY)	01295	SN74LS04N
A14U336	156-1722-00	B010100	B010169	IC,DIGITAL:FTTL,GATE;HEX INV;74F04,DIP14.3	04713	MC74F04N
A14U336	156-0385-00	B010170		IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04 (3001GPX ONLY)	01295	SN74LS04N
A14U338	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U338	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U338	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U339	160-8763-00	B010249		IC,DIGITAL:STTL,PLD;16L8,PRGM 156-1809-03 (2505 ONLY)	80009	156180903
A14U339	160-8763-00	B020100		IC,DIGITAL:STTL,PLD;16L8,PRGM 156-1809-03 (3001MPX ONLY)	80009	156180903
A14U339	160-8763-00	B030100		IC,DIGITAL:STTL,PLD;16L8,PRGM 156-1809-03 (3001HSM ONLY)	80009	156180903
A14U340	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U340	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U340	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U345	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U345	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U345	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14U348	156-2972-00	B010100	B010248	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (2505 ONLY)	0JR04	TC511000AP-10
A14U348	156-2972-00	B010100	B019999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001MPX ONLY)	0JR04	TC511000AP-10
A14U348	156-2972-00	B010100	B029999	IC,MEMORY:CMOS,DRAM;1024K X 1, 120NS;511000 (3001HSM ONLY)	0JR04	TC511000AP-10
A14U350	156-2478-00			IC,PROCESSOR:CMOS,PERIPHERAL;RTC, CLOCK	34371	ICM7170CPG/IPG
A14U360	156-1746-00			IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A14U365	156-0385-00			IC,DIGITAL:LSTTL,GATES;HEX INV;74LS04	01295	SN74LS04N
A14U370	156-0381-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT XOR	01295	SN74LS86AN
A14U375	156-0388-00			IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D W/SET &	01295	SN74LS74AN
A14U380	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U385	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A14U400	160-5952-01			MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-01
A14U410	160-5085-02	B010100	B010113	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-02
A14U410	160-5085-03	B010114		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001MPM ONLY)	80009	160-5085-03
A14U410	160-5085-02	B010100	B010174	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-02
A14U410	160-5085-03	B010175	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-03
A14U410	160-5085-04	B020100	B049999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-04
A14U410	160-5085-05	B050100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001MPX ONLY)	80009	160-5085-05
A14U410	160-5085-03	B010100	B010248	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-03
A14U410	160-5085-04	B010249	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-04
A14U410	160-5085-05	B020100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (2505 ONLY)	80009	160-5085-05
A14U410	160-5085-03	B010100	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-03
A14U410	160-5085-04	B030100	B059999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-04
A14U410	160-5085-05	B060100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001HSM ONLY)	80009	160-5085-05
A14U410	160-5085-04	B010100	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-04
A14U410	160-5085-05	B020100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001GPX ONLY)	80009	160-5085-05
A14U415	160-5086-02	B010100	B010113	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-02
A14U415	160-5086-03	B010114		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001MPM ONLY)	80009	160-5086-03
A14U415	160-5086-02	B010100	B010174	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-02
A14U415	160-5086-03	B010175	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-03
A14U415	160-5086-04	B020100	B049999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A14U415	160-5086-05	B050100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001MPX ONLY)	80009	160-5086-05
A14U415	160-5086-03	B010100	B010248	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-03
A14U415	160-5086-04	B010249	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A14U415	160-5086-05	B020100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (2505 ONLY)	80009	160-5086-05
A14U415	160-5086-03	B010100	B029999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-03
A14U415	160-5086-04	B030100	B059999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A14U415	160-5086-05	B060100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001HSM ONLY)	80009	160-5086-05
A14U415	160-5086-04	B010100	B019999	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-04
A14U415	160-5086-05	B020100		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3001GPX ONLY)	80009	160-5086-05

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14U420	156-2174-00			IC,PROCESSOR:NMOS,MICROPROCESSOR;16-BIT	04713	MC68010RC12
A14U430	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U435	156-1740-00	B010100	B010248	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER, (2505 ONLY)	34335	AM2966PC
A14U435	156-1740-00	B010100	B019999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER, (3001MPX ONLY)	34335	AM2966PC
A14U435	156-1740-00	B010100	B029999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER, (3001HSM ONLY)	34335	AM2966PC
A14U438	156-0467-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NAND	01295	SN74LS38N
A14U440	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U465	156-0392-00			IC,DIGITAL:LSTTL,FLIP FLOP;QUAD D W/CLR	01295	SN74LS175N
A14U470	156-0383-00			IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT NOR	01295	SN74LS02N
A14U475	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U480	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A14U485	156-0956-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV	01295	SN74LS244N3
A14U500	156-2782-00			IC,LINEAR:BIPOLAR,VOLTAGE REGULATOR	27014	LM337H
A14U513	156-1373-00			IC,DIGITAL:LSTTL,BUFFER/DRIVER;QUAD,	01295	SN74LS125AN
A14U515	156-1998-00			IC,DIGITAL:ALSTTL,FLIP FLOP;OCTAL D-TYPE	01295	SN74ALS273N
A14U518	160-4089-00			MICROCKT,DGTL:CMOS,GLUE ARRAY,PRGM3.5K	61892	UPD65042S-326
A14U525	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U528	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U535	156-1740-00	B010100	B010248	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (2505 ONLY)	34335	AM2966PC
A14U535	156-1740-00	B010100	B019999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (3001MPX ONLY)	34335	AM2966PC
A14U535	156-1740-00	B010100	B029999	IC,DIGITAL:TTL,BUFFER;OCTAL BUS DRIVER (3001HSM ONLY)	34335	AM2966PC
A14U536	156-3001-00	B010249		IC,DIGITAL:TTL,BUFFER/DRIVER;11-BIT DYNAMIC (2505 ONLY)	34335	AM2976PC
A14U536	156-3001-00	B020100		IC,DIGITAL:TTL,BUFFER/DRIVER;11-BIT DYNAMIC (3001MPX ONLY)	34335	AM2976PC
A14U536	156-3001-00	B030100		IC,DIGITAL:TTL,BUFFER/DRIVER;11-BIT DYNAMIC (3001HSM ONLY)	34335	AM2976PC
A14U538	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A14U545	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	4T165	UPD43256AC-12L
A14U550	156-1737-00			IC,PROCESSOR:MOS,PERIPHERAL;DUART,SCRN;2681	18324	SCN2681AC1 N40 OR I40
A14U555	156-1746-00			IC,DIGITAL:FTTL,MUX/ENCODER;8-TO-1 DATA	04713	MC74F151 N OR J
A14U558	156-0878-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A14U605	156-0631-00			IC,DIGITAL:ECL,GATE;QUAD 2-INPUT OR/NOR	04713	MC10101(L OR P)
A14U610	156-2142-00			IC,DIGITAL:ECL,COUNTER;4-BIT BINARY;10H016	04713	MC10H016(P OR L)
A14U635	156-0469-00			IC,DIGITAL:LSTTL,DEMUX/DECODER;3-TO-8	01295	SN74LS138 (N OR J)
A14U655	156-3053-00			IC,DIGITAL:ACMOS,GATE;QUAD 2-INPUT NAND	27014	74AC00PC
A14U660	156-0878-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE	04713	MC1489P
A14U700	156-3349-00			IC,DIGITAL:ACMOS,FLIP FLOP;HEX D-TYPE,CLEAR	27014	74AC174PC
A14U705	156-2350-00			IC,DIGITAL:ECL,TRANSLATOR;QUAD ECL-TO-TTL	04713	MC10H350 P OR L
A14U708	156-3060-00			IC,DIGITAL:ACMOS,FLIP FLOP;DUAL D-TYPE	27014	74AC74PC
A14U710	156-1639-00			IC,DIGITAL:ECL,FLIP FLOP;DUAL MASTER-SLAVE	04713	MC10H131(P OR L)
A14U713	156-2540-00			IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT NAND	18324	N74F38 N OR F
A14U715	156-1111-00			IC,DIGITAL:LSTTL,TRANSCEIVER;OCTAL NONINV	01295	SN74LS245N
A14U720	160-4091-00			MICROCKT,DGTL:CMOS,COMMUNICATION ARRAY,3.5K	61892	UPD65031S349
A14U730	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U735	156-1611-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE;74F74	04713	MC74F74N
A14U745	160-4090-00			MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM10K	61892	UPD65101S143
A14U750	156-0879-00			IC,DIGITAL:BIPOLAR,QUAD RS-232 LINE DRIVER	04713	MC1488P
A14U753	156-1226-00			IC,LINEAR:BIPOLAR,COMPARATOR;DUAL,OPEN	64155	LM319N
A14U836	156-3110-00			IC,DIGITAL:HCMOS,BUFFER;NONINV OCTAL, LINE	27014	MM74HC244N

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A14W312	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A14W465	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A14W860	----- -----			CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2 (SEE FIG 2-27 RMPL)	80009	175-6657-00
A14Y455	158-0305-00			XTAL UNIT,QTZ:32.768 MHZ,0.001%,CL=9PF	51791	FCX-1V
A14Y600	158-0106-00			XTAL UNIT,QTZ:100MHZ,+/-0.0025%	75378	HC42/U
A14YG190	119-1427-01			XDCR,AUDIO:1-4.2KHZ,30MA,6V	63791	QMB-06
A14YG610	119-3765-00			OSCILATOR,RF:40.045MHZ	61429	F1100H-40.045MHZ

1 OF 2 PUNCH: 3-HOLE

PLEASE INSERT 28 FOLDED 11 X 17 Z-FOLD(S) HERE

PART NUMBER: 070-7413-03 DATE: 6-25-98

1	1	DIA. & CIR. *FIG. 11-1
1	2	FIG. 11-2 *FIG. 11-3
1	3	FIG. 11-4 *FIG. 11-5
1	4	SCHEM 1 of 21 *BLANK
1	5	2 of 21 *BLANK
1	6	3 of 21 *BLANK
1	7	4 of 21 *BLANK
1	8	5 of 21 *BLANK
1	9	5A of 21 *BLANK
1	10	6 of 21 *BLANK
1	11	6A of 21 *BLANK
1	12	7 of 21 *BLANK
1	13	8 of 21 *BLANK
1	14	9 of 21 *BLANK
1	15	10 oif 21 *BLANK
1	16	11 of 21 *BLANK
1	17	12 of 21 *BLANK
1	18	13 of 21 *BLANK
1	19	14A of 21 *BLANK
1	20	14B of 21 *BLANK
1	21	14C of 21 *BLANK
1	22	15 of 21 *BLANK
1	23	16 of 21 *BLANK
1	24	17 of 21 *BLANK
1	25	18 of 21 *BLANK
1	26	19 of 21 *BLANK
1	27	20 of 21 *BLANK
1	28	21 of 21 *BLANK
2	29	EXPLODED FIG. 1 *BLANK
2	30	FIG. 2 *BLANK

Section 12
REPLACEABLE MECHANICAL PARTS

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. service center or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If a part you order has been replaced with a different or improved part, your local Tektronix service center or representative will contact you concerning any change in the part number.

Module Servicing

Change information, if any, is located at the rear of this manual. Your module can be serviced by selecting one of the following three options:

- **Module Exchange.** In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-835-9433.
- **Module Repair and Return.** You may ship your module to us for repair, after which we will return it to you.
- **New Modules.** You may purchase new replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all the information you need for ordering replacement parts.

Component Number (column 1)

Indentifies the fiqure and index number used on the mechanical exploded view.

Tektronix Part Number (column 2)

Indicates part number to be used when ordering replacement part from Tektronix.

Serial Number (columns 3 & 4)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number indicates part is good for all serial numbers.

Name and Description (column 5)

In the Parts List, an Item Name is separated from the description by a colon(:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

Mfr. Code (column 6)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

Mfr. Part Number (column 7)

Indicates actual manufacturer's part number.

Item Names

In the Replaceable Parts List, an Item Name is separated from the description by a colon(:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, U.S. Federal Cataloging Handbook H6-1 can be used where possible.

Indentation System

This parts list is indented to show the relationship between items. The following example is for the indentation system used in the Description column:

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
    Detail Part of Assembly and/or Component
    Attaching parts for Detail Part
        Parts of Detail Part
        Attaching parts for Parts of Detail Part

Attaching parts always appear at the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. Attaching parts must be purchased separately, unless otherwise specified.

Abbreviations

Abbreviations conform to American National Standards Institute (ANSI) standard Y1.1.

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV	1818 CHRISTINA ST	ROCKFORD IL 61108
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
0J260	COMTEK MANUFACTURING OF OREGON	PO BOX 4200	BEAVERTON OR 97076-4200
0KB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125-4632
1Y013	ACACIA/DEANCO	3101 SW 153RD DRIVE	BEAVERTON OR 97006
22152	NASHUA CORP	4402 N 23RD ST	OMAHA NE 68111
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR	FRANKLIN IN 46131
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532-1613
2K262	BOYD CORP	6136 NE 87th AVE	PORTLAND OR 97220
30817	INSTRUMENT SPECIALTIES CO INC	EXIT 53 RT 80	DELAWARE WATER GAP PA 18327
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
5Y400	TRIAX METAL PRODUCTS INC	1800 216TH AVE NW	HILLSBORO OR 97124-6629
61058	MATSUSHITA ELECTRIC CORP OF AMERICA PANASONIC INDUSTRIAL CO DIV	ONE PANASONIC WAY PO BOX 1502	SECAUCUS NJ 07094-2917
62559	SCHROFF INC	170 COMMERCE DR	WARWICK RI 02886-2430
65249	BOGEN COMMUNICATIONS INC	50 SPRING STREET	RAMSEY NJ 07446
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
78189	ILLINOIS TOOL WORKS INC	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
TK1471	PHOENIX CONTACT INC	1900 GREENWOOD ST	HARRISBURG PA 17104
TK2265	TEKTRONIX INC	PO BOX 1000	WILSONVILLE OR 97070-1000
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY	VANCOUVER WA 98601

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
1 -1	672-1304-00	B010100	B010154	1	CIRCUIT BD ASSY:MPU	80009	672-1304-00
	671-0058-00	B010100	B010154	1	.CIRCUIT BD ASSY:MPU	80009	671-0058-00
	671-0058-01	B010155	B010164	1	CIRCUIT BD ASSY:MPU	80009	671-0058-01
	671-0058-02	B010165	B010166	1	CIRCUIT BD ASSY:MPU	80009	671-0058-02
	671-0058-03	B010167	B010183	1	CIRCUIT BD ASSY:MPU	80009	671-0058-03
	671-0058-04	B010184	B010196	1	CIRCUIT BD ASSY:MPU	80009	671-0058-04
	671-0058-06	B010197	B010223	1	CIRCUIT BD ASSY:MPU	80009	671-0058-06
	671-0058-07	B010224	B010224	1	CIRCUIT BD ASSY:MPU	80009	671-0058-07
	671-0058-09	B010225	B020114	1	CIRCUIT BD ASSY:MPU	80009	671-0058-09
	671-0058-10	B020115	B020184	1	CIRCUIT BD ASSY:MPU	80009	671-0058-10
	671-0058-11	B020185	B020299	1	CIRCUIT BD ASSY:MPU	80009	671-0058-11
	671-0058-12	B020300	B020303	1	CIRCUIT BD ASSY:MPU	80009	671-0058-12
	671-0058-13	B020304	B029999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-13
	671-0058-14	B030100		1	CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	671-0058-14
	671-0058-03	B010100	B010173	1	CIRCUIT BD ASSY:MPU	80009	671-0058-03
	671-0058-04	B010174	B010220	1	CIRCUIT BD ASSY:MPU	80009	671-0058-04
	671-0058-05	B010221	B010224	1	CIRCUIT BD ASSY:MPU	80009	671-0058-05
	671-0058-06	B010225	B010255	1	CIRCUIT BD ASSY:MPU	80009	671-0058-06
	671-0058-07	B010256	B010345	1	CIRCUIT BD ASSY:MPU	80009	671-0058-07
	671-0058-08	B010346	B010475	1	CIRCUIT BD ASSY:MPU	80009	671-0058-08
	671-0058-09	B010476	B010794	1	CIRCUIT BD ASSY:MPU	80009	671-0058-09
	671-0058-10	B010795	B029999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-10
	671-0058-11	B030100	B050276	1	CIRCUIT BD ASSY:MPU	80009	671-0058-11
	671-0058-12	B050277	B060164	1	CIRCUIT BD ASSY:MPU	80009	671-0058-12
	671-0058-13	B060165	B069999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-13
	671-0058-14	B070100		1	CIRCUIT BD ASSY:MPU (3002 ONLY)	80009	671-0058-14
-2	131-3975-00			1	.CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR	22526	65496-019
-3	131-4037-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 4,0.2 CT	00779	641737-1
-4	131-3976-00			1	.CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR	22526	65496-001
-5	131-2215-01			1	.CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR	22526	65496-025
-6	131-4262-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.156	27264	26-48-2056
-7	131-0608-00			29	.TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025	22526	48283-036
-8	131-3969-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.2 CT	TK1471	1748222
-9	136-0755-00			2	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 14,28 POS (USED FOR U410 & U415)	09922	DILB28P-108
-10	253-0135-00			AR	.PLASTIC STRIP:VINYL FOAM,0.062 X 0.5	22152	ORDER BY DESCRIPTION
-11	174-0595-00	B010100	B010223	1	.CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON (2510 ONLY)	1Y013	62908
	174-0595-01	B010224		1	.CA ASSY,SP,ELEC:26,28 AWG,4.0 L,RIBBON (2510 ONLY)	1Y013	62908
	174-0595-00	B010100	B010345	1	.CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON (3002 ONLY)	1Y013	62908
	174-0595-01	B010346		1	.CA ASSY,SP,ELEC:26,28 AWG,4.0 L,RIBBON (3002 ONLY)	1Y013	62908
-12	136-0849-00			1	.SKT,PL-IN ELEK:PGA,MOT 68000;68 POS,10 X 1 (USED FOR U420)	00779	916220-2
-13	386-5598-00			1	.STIF,CIRCUIT BD:	0J260	386-5598-00
-14	136-0757-00	B010100	B020184	1	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,40 POS (2510 ONLY)	09922	DILB40P-108
	136-0757-00	B010100	B029999	1	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,40 POS (3002 ONLY)	09922	DILB40P-108
-15	352-0843-00			1	.HOLDER,BATTERY:LITHIUM,3V,150MA	65249	BH906
-16	----- -----			1	.BATTERY,DRY:3V,150MAH,BUTTON CELL (SEE A1BT275 REPL)	61058	BR2325
-17	407-3510-00			1	.BRACKET,CONN:COMM PACK,ALUMINUM	5Y400	407-3510-00
-18	211-0147-00			2	.SCREW,MACHINE:4-40 X 0.250,PNH,SST	0KB01	ORDER BY DESCRIPTION
-19	131-3947-00			1	.CONN,RCPT,ELEC:SNAP,20 CONTACT	00779	2-583900-8
-20	211-0315-00			2	.SCR,ASSEM WSHR:4-40 X 0.437,PHN,STL CD PL	78189	ORDER BY DESCRIPTION
-21	407-3502-00			1	.BRKT,COMM PACK:ALUMINUM	0J260	407-3502-00

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
1 -22	211-0661-00	B010100	B010196	4	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (2510 ONLY)	01536	821-01655-024
	211-0661-00	B010197		2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (2510 ONLY)	01536	821-01655-024
	211-0661-00	B010100	B010220	4	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (3002 ONLY)	01536	821-01655-024
	211-0661-00	B010221		2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (3002 ONLY)	01536	821-01655-024
-23	386-6064-00	B010197		1	.STIF,CKT BD:COMMPACK,BRACKET (2510 ONLY)	2K262	386-6064-00
	386-6064-00	B010221		1	.STIF,CKT BD:COMMPACK,BRACKET (3002 ONLY)	2K262	386-6064-00
-24	211-0244-00	B010197		2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CD PL (2510 ONLY)	01536	821-02775
	211-0244-00	B010221		2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CD PL (3002 ONLY)	01536	821-02775
-25	348-1180-00	B010197		1	.SHLD GSKT,ELEK:EMI (2510 ONLY)	30817	0493-0049-00
	348-1180-00	B010221		1	.SHLD GSKT,ELEK:EMI (3002 ONLY)	30817	0493-0049-00
-26	131-1003-00			1	.CONN,RF JACK:PCB,PELTOLA;FEMALE,STR,0.141	80009	131-1003-00
-26A	136-0252-07			1	.SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H	22526	75060-012
-27	175-6657-00			1	.CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
-28	407-3514-00	B010100	B010154	1	.BRKT,CONN MTG: (2510 ONLY)	0J260	407-3514-00
	407-3514-01	B010155		1	.BRKT,CONN MTG: (2510 ONLY)	5Y400	407-3514-01
	407-3514-01			1	.BRKT,CONN MTG: (3002 ONLY)	5Y400	407-3514-01
-29	211-0661-00			3	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL	01536	821-01655-024
-30	348-1086-00	B010100	B010164	2	.SHLD GSKT,ELEK:EMI GASKETING,CU-BE,3.75 L (2510 ONLY)	30817	97-542-19-3.75
-31	348-1088-00	B010100	B010164	1	.SHLD GSKT,ELEK:EMI,0.003,CU BE,9.0 L (2510 ONLY)	30817	97-542-19-9.00
-32	337-3624-00	B010165		1	.SHIELD,ELEC:CIRCUIT BD,BE-CU (2510 ONLY)	TK2265	337-3624-00
	337-3624-00			1	.SHIELD,ELEC:CIRCUIT BD,BE-CU (3002 ONLY;NOT USED IN 3001)	TK2265	337-3624-00
-33	131-1171-00			1	.CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR364-1
-34	131-3378-00			1	.CONN,RF JACK:BNC,;50 OHM,FEMALE,RTANG	00779	227677-1
-35	220-0497-00			2	.NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	73743	ORDER BY DESCRIPTION
-36	210-1039-00			1	.WASHER,LOCK:0.521 ID,INT,0.025 THK,SST	0KB01	1224-02-00-0541C
-37	210-0845-00			1	.WASHER,FLAT:0.5 ID X 0.625 OD X 0.02,STL	12327	ORDER BY DESCRIPTION
-38	131-3395-00			1	.CONN,DSUB:PCB,,;MALE,RTANG,25 POS,0.318 PC	00779	747842-4
-39	131-0890-00			2	.SCREW LOCK:4-40 X 0.312 L HEX HD,STLCD PL	0KB01	131-0890-00
-40	131-4495-00			2	.CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	10226-52B2VE
-41	211-0402-00			4	.SCREW,MACHINE:M2.5 X 0.45 X 8,SLOTTED	62559	21100-140
-42	671-0980-00	B010100	B010154	1	.CIRCUIT BD ASSY:VIDEO FILTER389-0277-XX (2510 ONLY)	80009	671-0980-00

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
2 -1	671-0058-51	B010100	B010113	1	CIRCUIT BD ASSY:MPU	80009	671-0058-51
	671-0058-52	B010114	B010125	1	CIRCUIT BD ASSY:MPU	80009	671-0058-52
	671-0058-53	B010126	B010128	1	CIRCUIT BD ASST:MPU	80009	671-0058-53
	671-0058-54	B010129		1	CIRCUIT BD ASSY:MPU (3001MPM ONLY)	80009	671-0058-54
	671-0058-51	B010100	B010174	1	CIRCUIT BD ASSY:MPU	80009	671-0058-51
	671-0058-52	B010175	B010190	1	CIRCUIT BD ASSY:MPU	80009	671-0058-52
	671-0058-53	B010191	B010209	1	CIRCUIT BD ASST:MPU	80009	671-0058-53
	671-0058-54	B010210	B019999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-54
	671-0058-55	B020100	B029999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-55
	671-0058-56	B030100	B040104	1	CIRCUIT BD ASSY:MPU	80009	671-0058-56
	671-0058-57	B040105	B049999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-57
	671-0058-58	B050100		1	CIRCUIT BD ASSY:MPU (3001MPX ONLY)	80009	671-0058-58
	671-0058-52	B010100	B010140	1	CIRCUIT BD ASSY:MPU	80009	671-0058-52
	671-0058-53	B010141	B010159	1	CIRCUIT BD ASST:MPU	80009	671-0058-53
	671-0058-54	B010160	B029999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-54
	671-0058-55	B030100	B039999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-55
	671-0058-56	B040100	B049999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-56
	671-0058-57	B050100	B059999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-57
	671-0058-58	B060100		1	CIRCUIT BD ASSY:MPU (3001HSM ONLY)	80009	671-0058-58
	671-0058-56	B010100	B010169	1	CIRCUIT BD ASSY:MPU	80009	671-0058-56
	671-0058-57	B010170	B019999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-57
	671-0058-58	B020100		1	CIRCUIT BD ASSY:MPU (3001GPX ONLY)	80009	671-0058-58
	671-0058-54	B010100	B010248	1	CIRCUIT BD ASSY:MPU	80009	671-0058-54
	671-0058-55	B010249	B010281	1	CIRCUIT BD ASSY:MPU	80009	671-0058-55
	671-0058-56	B010282	B010287	1	CIRCUIT BD ASSY:MPU	80009	671-0058-56
	671-0058-57	B010288	B019999	1	CIRCUIT BD ASSY:MPU	80009	671-0058-57
	671-0058-58	B020100		1	CIRCUIT BD ASSY:MPU (2505 ONLY)	80009	671-0058-58
-2	131-3975-00			1	.CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR	22526	65496-019
-3	131-4037-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 4,0.2 CT	00779	641737-1
-4	131-3976-00	B010160		1	.CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001HSM ONLY)	22526	65496-001
	131-3976-00	B010129		1	.CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001MPM ONLY)	22526	65496-001
	131-3976-00	B010210		1	.CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (3001MPX ONLY)	22526	65496-001
	131-3976-00			1	.CONN,HDR::PCB,;MALE,RTANG,2 X 5,0.1 CTR (2505 ONLY)	22526	65496-001
-5	131-2215-01	B010160		1	.CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001HSM ONLY)	22526	65496-025
	131-2215-01	B010129		1	.CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001MPM ONLY)	22526	65496-025
	131-2215-01	B010210		1	.CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (3001MPX ONLY)	22526	65496-025
	131-2215-01			1	.CONN,HDR:PCB,;MALE,RTANG,2 X 20,0.1 CTR (2505 ONLY)	22526	65496-025
-6	131-4262-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.156	27264	26-48-2056
-7	131-0608-00			29	.TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025	22526	48283-036
-8	131-3969-00			1	.CONN,HDR PWR::PCB,;MALE,RTANG,1 X 5,0.2 CT	TK1471	1748222
-9	337-3673-00			1	.SHIELD,ELEC:6.25 X 6.5,POLYESTER,CLEAR	2K262	337-3673-00
-10	196-3285-00			1	.LEAD,ELECTRICAL:26 AWG,3.0 L	TK2469	196-3285-00
-11	407-3916-00			1	.BRKT,CKT BD:ALUMINUM,MPU MTG	5Y400	407-3916-00
-12	211-0658-00			3	.SCR,ASSEM WSHR:6-32 X 0.312,PNH,STL,POZ	78189	S51-060545-0X
-13	136-0755-00			2	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 14,28 POS (USED FOR U410 & U415)	09922	DILB28P-108
-14	253-0135-00			AR	.PLASTIC STRIP:VINYL FOAM,0.062 X 0.5	22152	ORDER BY DESCRIPTION
-15	136-0849-00			1	.SKT,PL-IN ELEK:PGA,MOT 68000;68 POS,10 X 1 (USED FOR U420)	00779	916220-2

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
2 -16	386-5598-00			1	.STIF,CIRCUIT BD:	0J260	386-5598-00
-17	136-0757-00	B010100	B010248	1	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,40 POS (2505 ONLY)	09922	DILB40P-108
	136-0757-00	B010100	B019999	1	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,40 POS (3001MPX ONLY)	09922	DILB40P-108
	136-0757-00	B010100	B029999	1	.SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,40 POS (3001HSM ONLY)	09922	DILB40P-108
-18	352-0843-00			1	.HOLDER,BATTERY:LITHIUM,3V,150MA	65249	BH906
-19	----- -----			1	.BATTERY,DRY:3V,150MAH,BUTTON CELL (SEE A14BT275 REPL)	61058	BR2325
-20	407-3510-00			1	.BRACKET,CONN:COMM PACK,ALUMINUM	5Y400	407-3510-00
-21	211-0147-00			2	.SCREW,MACHINE:4-40 X 0.250,PNH,SST	0KB01	ORDER BY DESCRIPTION
-22	131-3947-00			1	.CONN,RCPT,ELEC:SNAP,20 CONTACT	00779	2-583900-8
-23	211-0315-00			2	.SCR,ASSEM WSHR:4-40 X 0.437,PHN,STL CD PL	78189	ORDER BY DESCRIPTION
-24	407-3502-00			1	.BRKT,COMM PACK:ALUMINUM	0J260	407-3502-00
-25	211-0661-00			4	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL	01536	821-01655-024
-26	131-1003-00			1	.CONN,RF JACK:PCB,PELTOLA;FEMALE,STR,0.141	80009	131-1003-00
-26A	136-0252-07			1	.SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H	22526	75060-012
-27	175-6657-00			1	.CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
-28	407-3421-00			1	.BRACKET,CONN:MOUNTING,ALUMINUM (USED IN 3001 ONLY)	5Y400	407-3421-00
-29	211-0661-00			1	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL	01536	821-01655-024
-30	210-3057-00	B010141		2	.WASHER,FLAT:0.17 ID X 0.375 OD X 0.03 THK, (3001MPM ONLY)	0KB01	LWNY-012NA-M
	210-3057-00	B010250		2	.WASHER,FLAT:0.17 ID X 0.375 OD X 0.03 THK, (3001MPX ONLY)	0KB01	LWNY-012NA-M
	210-3057-00	B020100		2	.WASHER,FLAT:0.17 ID X 0.375 OD X 0.03 THK, (3001HSM ONLY)	0KB01	LWNY-012NA-M
-31	344-0457-00	B010141		2	.CLIP,RETAINER:ALUMINUM (3001MPM ONLY)	5Y400	344-0457-00
	344-0457-00	B010250		2	.CLIP,RETAINER:ALUMINUM (3001MPX ONLY)	5Y400	344-0457-00
	344-0457-00	B020100		2	.CLIP,RETAINER:ALUMINUM (3001HSM ONLY)	5Y400	344-0457-00
-32	211-0661-00	B010100	B019999	2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (3001HSM ONLY)	01536	821-01655-024
	211-0244-00	B010141		2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CD PL (3001MPM ONLY)	01536	821-02775
	211-0661-00	B010100	B010140	2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (3001MPM ONLY)	01536	821-01655-024
	211-0244-00	B010250		2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CD PL (3001MPX ONLY)	01536	821-02775
	211-0661-00	B010100	B010249	2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,CD PL (3001MPX ONLY)	01536	821-01655-024
	211-0244-00	B020100		2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CD PL (3001HSM ONLY)	01536	821-02775
-33	131-1171-00			1	.CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR364-1
-34	131-3378-00			1	.CONN,RF JACK:BNC,;50 OHM,FEMALE,RTANG	00779	227677-1
-35	220-0497-00			2	.NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	73743	ORDER BY DESCRIPTION
-36	210-1039-00			1	.WASHER,LOCK:0.521 ID,INT,0.025 THK,SST	0KB01	1224-02-00-0541C
-37	210-0845-00			1	.WASHER,FLAT:0.5 ID X 0.625 OD X 0.02,STL	12327	ORDER BY DESCRIPTION
-38	131-3395-00			1	.CONN,DSUB:PCB,,;MALE,RTANG,25 POS,0.318 PC	00779	747842-4
-39	131-0890-00			2	.SCREW LOCK:4-40 X 0.312 L HEX HD,STLCD PL	0KB01	131-0890-00
-40	131-4495-00			1	.CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	10226-52B2VE
-41	211-0402-00			2	.SCREW,MACHINE:M2.5 X 0.45 X 8,SLOTTED	62559	21100-140
					OPTIONAL ACCESSORY		
	070-7413-02			1	MANUAL,TECH:SERVICE,MPU	80009	070-7413-02

2 OF 2 PUNCH: 3-HOLE

PLEASE INSERT 2 FOLDED 11 X 17 Z-FOLD(S) HERE

PART NUMBER: 070-7413-03 DATE: 6-25-98

1	1	DIA. & CIR. *FIG. 11-1
1	2	FIG. 11-2 *FIG. 11-3
1	3	FIG. 11-4 *FIG. 11-5
1	4	SCHEM 1 of 21 *BLANK
1	5	2 of 21 *BLANK
1	6	3 of 21 *BLANK
1	7	4 of 21 *BLANK
1	8	5 of 21 *BLANK
1	9	5A of 21 *BLANK
1	10	6 of 21 *BLANK
1	11	6A of 21 *BLANK
1	12	7 of 21 *BLANK
1	13	8 of 21 *BLANK
1	14	9 of 21 *BLANK
1	15	10 oif 21 *BLANK
1	16	11 of 21 *BLANK
1	17	12 of 21 *BLANK
1	18	13 of 21 *BLANK
1	19	14A of 21 *BLANK
1	20	14B of 21 *BLANK
1	21	14C of 21 *BLANK
1	22	15 of 21 *BLANK
1	23	16 of 21 *BLANK
1	24	17 of 21 *BLANK
1	25	18 of 21 *BLANK
1	26	19 of 21 *BLANK
1	27	20 of 21 *BLANK
1	28	21 of 21 *BLANK
2	29	EXPLODED FIG. 1 *BLANK
2	30	FIG. 2 *BLANK

Section 13
SIGNAL GLOSSARY

INTRODUCTION

This glossary provides an alphabetical listing and description of circuit board and module interconnect signals. Signal descriptions are also provided for all external interconnect signals and 68010 microprocessor input/output signals.

+REMOTE ON/OFF. Output signal from the MPU board to the Power Supply. A low signal switches the Power Supply on; a high signal switches the Power Supply off.

1MHZ. A 1 MHz clock from the 68010 to the Hard Disk Controller board where it clocks the RAM address counter.

1.81MHZ. The 1.81 MHz clock from the MPU board to the COMM pack

8MHZ. A free-running, 50% duty cycle clock used for internal timing of the floppy controller IC.

10MHZ. Processor clock from the MPU board's GLUE gate array.

40MHZ. Master clock oscillator frequency to GLUE gate array on MPU board.

1772_SELECT. The low-active select signal for the floppy controller IC.

A_LATCH. A latch signal from COMM pack interface to MPU board (reserved for future applications).

ABENABLE/. The low-active address buffer enable signal that enables the COMM pack address buffers.

ABR[0–12]. Data address lines between the TekLink gate array and TekLink RAM.

ACPK[O:15]. Data address lines between the COMM pack interface and the MPU board.

ALCH/. A low-active signal that latches the data address into a 16-bit COMM pack. This signal is used only when a 16-bit COMM pack is installed.

BAUDCLK. The communications rate control signal from the GLUE gate array that sets the data transfer rate for the Keyboard, host interface, and COMM pack.

BBA[01:16]. Sixteen bits of the buffered kernel address bus.

BBRW. This is the buffered KRW signal. Refer to KRW signal description.

BD[0:15]. Sixteen bits of the buffered kernel data bus.

BDTACK. Buffered data transfer acknowledge. See DTACK.

BERR/. Bus error input to the 68010. Informs the microprocessor that there is a problem with the cycle currently being executed. Problems may be a result of:

- Illegal access request as determined by a memory management unit
- Interrupt vector number acquisition failure
- Non-responding devices
- Other application dependent errors

BLDS/. Buffered lower data strobe. See **KLDS/.**

BUDS/. Buffered upper data strobe. See **KUDS/.**

BUN/. An active-low enable signal from the Glue gate array to the data/address bus buffers and the DTACK control circuit that allows the 68010 microprocessor to communicate with the Video gate array, TekLink gate array, hard disk drive.

CALENDARR/. Calendar read signal. The content of the addressed calendar register is read to the IOD data bus when this signal goes low.

CALENDARW/. Calendar write signal. The content of the IOD data bus is read to the addressed calendar register when this signal goes low.

CAS00 and CAS01 (2 Mbyte RAM). The buffered column address strobes. The falling edge of **CAS00** writes eight bits to the low order RAM; the falling edge of **CAS01** writes eight bits to the high order RAM.

CAS00, CAS01, CAS10, and CAS11 (4 Mbyte RAM). DRAM column address strobes. The falling edge of **CAS00** writes the addresses to the low-order byte for the lower 2 Mbyte bank of RAM. **CAS01** writes the addresses to the high-order byte for the lower 2 Mbyte bank of the RAM. **CAS10** writes the addresses to the low-order byte for the upper 2 Mbyte bank of the RAM. **CAS11** writes the addresses to the high-order byte for the upper 2 Mbyte bank of the RAM.

CAS1 and CAS2 (2 Mbyte RAM). Column address strobe from GLUE gate array to the column address strobe buffer.

CAS1, CAS2, CAS3, and CAS4 (4 Mbyte RAM). Column address strobes from GLUE gate array to the refresh decoder.

CLK. Clock signal from the Video gate array to the Flat Panel Display module. Used for timing data to the flat panel display.

CLK_TICK. An interrupt from the keyboard channel of the DUART to the interrupt multiplexer. Indicates that the keyboard input is about to change from using the keys to using the KNOB, and vice versa.

COM_IC_SELECT. A low-active enable signal from the MPU board's GLUE gate array, to the COMM pack interface.

COMINT. The TekLink gate array interrupt signal to the interrupt multiplexer.

COMPKIRQ. Input signal to the MPU board from a COMM pack. Used to interrupt the MPU's microprocessor.

CPURESET/. The microprocessor reset signal from the system reset circuit to the 68010 microprocessor.

CROM/. Bit 16 of the 16-bit COMM pack data address bus. When low-active from the MPU to the COMM pack interface it enables the MPU to read the COMM pack's ROM.

CTS. The clear to send signal from a connected RS-232C device to the MPU board.

CVWS. The Com (TekLink), video, and Winchester® Select signal. This signal goes active to enable the addressed device by activating the following signals:

D[0:7]. Data bits 0–7 between the COMM pack device and the MPU board.

DCD. Data carrier detect signal from the connected RS-232C device to the MPU board's host interface.

DEBUG_INT. Debug (NMI) interrupt signal from a remote test switch (ground closure).

DIRI and **DIRX.** Refer to *Signal Descriptions* under *Acquisition Module Interface* description in Section 4.

DRIVE SELECT 1/. Low-active output from Hard Disk Controller board to select the hard disk drive unit. This signal enables all other interface signal lines on the hard disk drive unit.

DRIVE_0 and DRIVE_1. Drive select signals from the MPU board to the floppy disk drives(s). DRIVE_0 is factory set to enable drive 0 only. **DRIVE_1** is reserved for future applications.

DSR. Data set ready signal from the connected RS-232C host to the MPU board's host interface circuits.

DTACK/. Data transfer acknowledge. This input to the 68010 indicates that a data transfer is completed. When the microprocessor recognizes **DTACK/** during a read cycle, data is latched in to the microprocessor, one clock cycle later and the bus cycle is terminated. When **DTACK/** is recognized during a write cycle, the bus cycle is terminated.

E0–E3 (Event Lines). Refer to *Signal Descriptions* under*Application Module Interface* description in Section 4.

ETRG. External trigger signal from TekLink gate array to external trigger level shift circuit. Causes SYSTRIG signal to go high-active. This signal is normally activated when running diagnostic test routines.

FC0–FC2. Function code outputs from the 68010 that initiate the state (user or supervisor) and the address space currently being accessed. The information indicated by the function code outputs is valid whenever address strobe (KAS/) is active.

FDSELEN. Floppy disk select enable. A low-active signal from the function select circuit to the floppy select latch. Latches floppy drive status bits from floppy drive into floppy select latch.

FLOPPY_DRQ. A high-active output from the floppy controller IC. Indicates that the chip's data register is full (on a read cycle) or empty (on a write operation).

FLOPPY_IRQ. A high-active output from the floppy controller IC. Normally set at the completion of any command or when resetting a read of the chip's status register

GBA[1–8]. The GLUE bus address bits 1–8.

HALT/. This bidirectional 68010 signal line causes the 68010 to stop at the completion of the current bus cycle. When halted as the result of using this input signal, all control signals are inactive and all three-state lines are put in their high-impedance state.

HALT_LED. Signal from the power control circuit to the diagnostic LED HALT indicator. Low-active indicates a microprocessor halt condition.

HARDDISKINT. An interrupt signal to the MPU board from the Hard Disk Controller board. When HARDDISKINT is asserted, it alerts the MPU that a hard-disk related command has terminated (either a normal termination or an aborted termination). HDDISKINT remains asserted until either the MPU reads the hard disk controller IC's status register to determine the result of the termination, or the MPU writes a new command into the controller's command register.

HDC. Hard disk controller enable signal. When the signal is active low, **HDC** indicates that the hard disk controller circuitry is being addressed.

HDDIR. Output signal from the Hard Disk Controller board to the hard disk drive unit. This signal determines the direction the head will move when the drive receives a **STEP/** pulse. When logic low, a **STEP/** pulse moves the heads toward the center of the disk (toward the higher number cylinders); when logic high, a **STEP/** pulse moves the heads toward the outer edge of the disk (toward the lower number cylinders).

HDINDEX/. Input to the Hard Disk Controller board from the hard disk drive unit. An index pulse is generated once for each revolution of the disk. (The leading edge of this pulse is referenced to a constant point on the rotating disk system.)

HDRDATA and **HDRDATA/**. The plus and minus data signals from the hard disk drive to the Hard Disk Controller board.

HDREADY/. Status signal input to the Hard Disk Controller board from the hard disk drive unit. This signal is active low when the drive is ready for reading or writing and all other control output lines are valid. **READY/** remains true until power off or until a drive error occurs.

HDSEL0/ and **HDSEL1/.** Outputs from the Hard Disk Controller board to the hard disk drive unit. These lines determine which head is used for a read or write operation, as follows:

Table 13-1
Head Selection

HDSEL0/	HDSEL1/	Head Number
High	High	0
High	Low	1
Low	High	2
Low	Low	3

HDSTEP/. Control signal output from the Hard Disk Controller board to the hard disk unit. Each low-active **HDSTEP** signal steps the read/write head one cylinder. (The direction of head movement is determined by **HDDIR/**.)

HDTRK0/. Status signal input from hard disk unit to Hard Disk Controller board. Signal is low-active whenever heads are positioned at cylinder 0.

HDWDATA and **HDWDATA/**. The plus and minus data signals from the Hard Disk Controller board to the hard disk drive unit.

HDWGATE/. Control signal output from the Hard Disk Controller board to the hard disk drive unit. When high, the drive can write data to the disk; when low, the drive can transfer (read) data to the Hard Disk Controller board.

HDWRFLT/. Fault status signal input to the Hard Disk Controller board from the hard disk drive unit. This signal goes true whenever one of the following conditions occurs:

- –5 V supply lower than 4.5 V and **HDWGATE/** is true.
- –12 V supply lower than 10.3 V
- **HDWGATE/** true but no write data transitions
- **HDWGATE/** true but no write current in head
- head center tap open circuit
- head input line open circuit
- head input line shorted to center tap
- head input line shorted to ground
- head input lines shorted together
- step pulse received while **HDWGATE/** is true

HS(OUT) and **HS(IN).** Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

HSYNC. Horizontal sync signal output from the MPU board to the CRT display unit. This signal synchronizes display operation to pixel data. Programmable parameters are: pulse width, duty cycle, and retrace interval.

INDEX. Status signal input to the MPU board from the floppy disk drive unit. The leading edge of this signal pulse is referenced to a constant point on the rotating disk system.

INTH. High-active interrupt high priority signal. Generated by the interrupt multiplexer and used together with **INTL** by the GLUE gate array to determine the priority of the interrupting device.

INTL. High-active interrupt low priority signal. Generated by the interrupt multiplexer and used together with **INTH** by the GLUE gate array to determine the priority of the interrupting device.

IO_RESET. One of the system reset signals. An active-high signal resets the GLUE gate array and the keyboard.

IOD[00:07]. Eight bits of the GLUE gate array's input/output data bus.

IORESET/. Active-low system reset signal that resets the diagnostic LEDs, Video gate array, floppy disk drive interface circuits, TekLink gate array, and the hard disk drive circuitry.

IP3. General purpose input signal to the DUART IC. Use is software-dependent.

IPL0/–IPL2/. Interrupt control signals input to the 68010. These signals indicate the encoded priority level of the device requesting an interrupt. The least significant bit is IPL0 and the most significant bit is IPL2. These lines remain stable until the microprocessor signals interrupt acknowledge (**FC0–FC2** are all high, and **KA[16:19]** are all high) to ensure that the interrupt is recognized.

IRQ. Interrupt request signal from keyboard and host DUART to interrupt multiplexer circuit. Goes active high with KBTRANINT to inform GLUE gate array that DUART has data to transmit to IOD data bus.

KA[01:24]. Kernel bus address lines.

KAS. Address strobe from 68010. Indicates that there is a valid address on the kernel (KA) address bus.

KBRECINT. Keyboard receive interrupt strobe to interrupt multiplexer circuit. High-active indicates to GLUE (via **INTL** and **INTH** outputs of interrupt multiplexer) that a byte of keyboard data is residing in DUART and is ready for placement on the IOD data bus.

KBTRANINT. Keyboard transmit interrupt strobe to interrupt multiplexer circuit. High-active indicates to the GLUE gate array (via **INTL** and **INTH** outputs of Interrupt Multiplexer) that the keyboard is able to accept data from off the IOD data bus via the keyboard's DUART channel.

KD[0:15]. The 16-bit bidirectional, three-state, data bus for the 68010 and associated MPU kernel circuits.

KEY.CLOCK. The 19.2 kHz clock by which data is clocked from the keyboard to the MPU's DUART chip.

KEY.COMD. Serial byte data from the MPU to the keyboard when MPU wishes to interrogate keyboard extended functions.

KILLPOWER. When grounded this line causes an interrupt, informing the microprocessor that a power-off cycle is in progress.

KLDS/. Kernel lower data strobe. Output signal from the 68010 that is used with **KUDS/** (kernel upper data strobe) and **KRW** signals to control the flow of data on the data bus.

KRW. Read/Write signal from the 68010. Used with **KLDS** and **KUDS** signals to control the flow of data on the data bus.

KUDS/. Kernel upper data strobe. Output signal from the 68010 that is used with the **KLDS** and **KRW** signals to control the flow of data on the data bus.

LBRW. Buffered read/write signal from GLUE gate array to floppy controller IC. A logic high on this inputs controls the placement of data on the **IOD[0–7]** data bus from the selected floppy controller register. A logic low causes a write operation to the selected register.

LED. A low-to-high transition on this line clocks data bits **KD[0:7]** into the diagnostic LED buffers. A steady logic high allows power control circuit to be strobed (under program control) by address line **KA[23]**; this delays the power down cycle as long as strobe action continues.

LORA[0:9]. Dynamic RAM address lines 0–9.

LOW BATTERY. Input signal to the MPU board from the 12 V Battery Power Supply. It signals a low battery condition.

LOW BATTERY/POWER FAIL RETURN. Return line for **LOW BATTERY** and **POWER FAIL** signal lines.

LSIO. Signal line used to active a device enable signal for the selected 8-bit device.

M[0–15]. Video RAM data bits.

MCK and **MCK/.** Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

MOTOR ON/. An active low signal from the MPU board to the floppy disk drive unit that starts the spindle motor.

OEL. Output enable strobe. A low-active condition causes the addressed data to be read from the TekLink RAM onto the **R[0:15]** data bus.

PACK/. The low-active COMM pack device select signal from the DTACK device enable circuit.

PACKREAD. Low-active COMM pack read signal from the GLUE gate array. Causes data from COMM pack to be placed on the **D[0:7]** data bus.

PACKWRITE. Low-active COMM pack write signal from the Glue gate array. Causes data to be strobed from off the **BD[00:07]** data bus to the **D[0:7]** data bus.

PAKINT. COMM pack interrupt signal to interrupt multiplexer. Goes high-active when either **PK/** or **COMPKIRQ** go high.

PFINT. Power fail interrupt signal from the power supply to the MPU board. This line goes active when the power supply loses mains voltage.

PK/. COMM pack signal. Used to reset **PAKINT** signal. Whether high or low-active depends on status of **COMPKIRQ** signal. Normally low-active.

PTR1, PTR2, PRT3. Pointer. **PTR1** and **PTR2** are 10 MHz clocks. **PTR3** is a 5 MHz clock. These signals are used by the GLUE gate array, in conjunction with the **INTL** and **INTH** signals from the interrupt multiplexer, to determine the priority of the interrupting device.

R[0:5]. Data bus between TekLink gate array and TekLink RAM.

RA[0:15]. Video RAM address lines.

RAS00 and **RAS01** (2 Mbyte RAM). The buffered **RASL** signal. The falling edge of **RAS00** writes 8 bits to the low order RAM; the falling edge of **RAS01** writes 8 bits to the high order RAM.

RAS0 and **RAS1** (4 Mbyte RAM). Row address strobes. The falling edge of **RAS0** writes the row addresses into the lower 2 Mbyte bank of the RAM. The falling edge of RAS1 WRITES the row addresses into the upper 2 Mbyte bank of the RAM.

RASL (2 Mbyte RAM). Low-active row address strobe from the GLUE gate array. This signal inputs to separate buffers; thereby generating the RAS00 and RAS01 dynamic RAM address control signals.

RASL and **RASH** (4 Mbyte RAM). Low-active row address strobes from the GLUE gate array. These signals are used by the refresh decoder to determine if a refresh cycle (both RASL and RASH low at the same time) is needed. RAS0 and RAS1 are derived from these signals.

RDATA. The keyboard data line that transfers keyboard data bit-serially from the keyboard to the MPU board.

RDN. DUART read strobe. When low, the contents of the addressed DUART register are presented to the **BD[0:7]** data bus. A read cycle begins on the falling edge of **RDN.**

READY/. Status signal input to the MPU board from the floppy disk drive unit. This signal is true when the floppy disk drive is ready for reading or writing and all other drive control output lines are valid.

RECDATA. Serial data from the keyboard to the MPU board.

RECINT. Receive interrupt. A high-active signal from the DUART signalling the MPU that a byte of host data is in the DUART's host channel.

REMOTE ON/OFF. Ground potential on this signal line causes power supply to turn on.

RESET. High-active reset signal to power supply control circuit. Causes **HALT/** and **HALT_LED** signals to become active low and high, respectively.

RESETLED. Reset diagnostic LEDs. This signal, from the system reset circuit, goes active high whenever the MPU is in a reset condition. Signal activates the **RESET** indicator on the diagnostic LEDs.

RID[0:15]. Dynamic RAM data lines.

RMRW. Dynamic RAM read/write signal line. A logic high signifies read mode; a logic low sets write mode.

ROM. Low-active read only memory chip enable signal from GLUE gate array.

RUN. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

RW0/ and RW1/. Read and Write strobes for low and high byte RAM, respectively. Low-active sets write mode. High-active sets read mode.

SCK and SCK/. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

SD. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

SEEKCOMP/. Input signal to the Hard Disk Controller board from the hard disk drive unit. Goes low-active at the end of a seek operation, indicating that the heads are positioned at the desired cylinder.

SIDE_I/O. Output signal from the MPU board to the floppy disk drive unit. This signal selects the disk side that is opposite from the side currently selected.

SIZE_SELECT_8/16. A data path selector signal from the COMM pack interface to the MPU board. Low level selects 8-bit path width; high level selects 16-bit path width (16-bit path reserved for future applications).

STDS. Standard data strobe used to activate individual decoded data strobes for 8-bit peripherals.

STEP/. Head control signal from the MPU to the floppy disk drive. The number of pulses determines the amount of head movement. (The direction of head movement is determined by the **DIRECTION** signal.)

SYSTRIG. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

THERM. Thermal signal. A thermal (over-temperature condition on an acquisition module places a ground potential on this line. This causes the Power Supply to shut down via the power supply control circuitry.

TLGA_SELECT/. TekLink gate array select line. A low-active signal enables (selects) the TekLink gate array.

TLGA_SELECT. Enables the TekLink gate array.

TR_0/. Status input signal from the floppy disk drive unit to the MPU board. This signal is true when the heads are positioned at Track 00.

TRANDATA. Serial byte data from the MPU to a connected RS-232C host/device.

TRANINT. DUART host transmit interrupt signal. The DUART sets this line active high when it is ready to receive data from the buffer data bus **BD[00:07].**

TRIG IN. An ECL trigger In signal at J850 activates the SYSTRIG signal, thus synchronizing the MPU application to an external trigger source.

TRIG OUT. ECL trigger out signal to J950. This signal is useful when it is necessary to synchronize the functions of other triggered sources to that of the MPU application.

VGA_SELECT/. Video gate array select signal. A low-active signal enables (selects) the Video gate array.

VGA_SELECT. Enables the Video gate array.

VID0–VID3. Video data from MPU to a display module. If display module is a flat panel, then **VID0–VID3** provide ON/OFF data for four pixels in series on a horizontal display line. (**VID0** is left-most pixel; **VID3** is right-most pixel.) If display module is a color CRT monitor, then **VID1** = blue; **VID2** = Green; and **VID3** = Red (VID0 not used with color CRT). If the display module is a monochrome CRT, then **VID0** high = white and **VID0** low = black (**VID1**, **VID2**, and **VID3** not used with monochrome CRT).

VIDEO_INT. Video interrupt signal from the Video gate array to the interrupt multiplexer circuit.

VSYNC. Vertical sync output from the MPU board to a display unit. This signal synchronizes display operation to pixel data. Programmable parameters are: pulse width, duty cycle, and retrace interval.

WEL. Write-enable line. A low-active condition causes data on the **R[0:15]** data bus to be written into TekLink RAM.

WGATE. Write data control signal from the MPU board to the floppy disk drive unit. When low-active, the floppy disk drive unit can write data to the disk. When high-active, the floppy disk drive unit can transfer (read) data to the MPU.

WPROTECT/. Control signal from the floppy disk drive unit to the MPU board. Signal goes low-active when there is a write-protected disk in the drive. Also goes low if Vcc drops below the required level for write protection.

WRDATA. Write data from the MPU board to the floppy disk drive unit.

WRITE/. The buffered **PACKWRITE** signal from the GLUE gate array to the COMM pack unit.

WRN. The DUART write strobe. When low, the contents of the **BD[00:07]** data bus are loaded into the address DUART register. Transfer occurs on the rising edge of **WRN**.

Appendix A
KERNEL TEST MONITOR

INTRODUCTION

The Test Monitor resides in ROM and is useful for low-level troubleshooting of the 68010 microprocessor and associated circuitry. There are two versions of the Monitor: a RAM and a RAM-less version. The information presented here summarizes the functionality and command set of the Test Monitor. In addition, instructions are provided on how to enter the monitor and how to input and output test data.

FUNCTIONAL OVERVIEW

Test Monitor functions can be grouped as follows:

Execution Controls

Execution control commands include instruction single-stepping, instruction-stream breakpoints, and breakpoints.

pSOS Queries

pSOS query commands produce formatted displays of status information on key system resources, such as available memory, related data structures (such as queues and lists), and objects (such as user processes and message exchanges).

pSOS Service Calls

Relevant pSOS system service calls (such as suspend_process) may be invoked directly as Test Monitor commands. They may also be used to manipulate, coerce, isolate, or simulate system execution and activity.

Data Input/Output

All data input/output is through either an RS232 COMM pack or the RS232 host port on the MPU board. The default port is the 1200C01 COMM pack. If an RS232 COMM pack (1200C01) is not installed, then the Monitor uses the host RS232 port. You can switch ports using the ALTERNATE command, if desired. (See *ALTERNATE* command.)

All ports are set at 9600 baud, 8 bits per character, no parity (non-selectable).

One of the above ports must be connected to a dumb terminal. You can use the other port to send commands to an host computer and to accept downloaded S-records from the computer. Thus, the two communication configurations shown in Figure A-1 are possible.

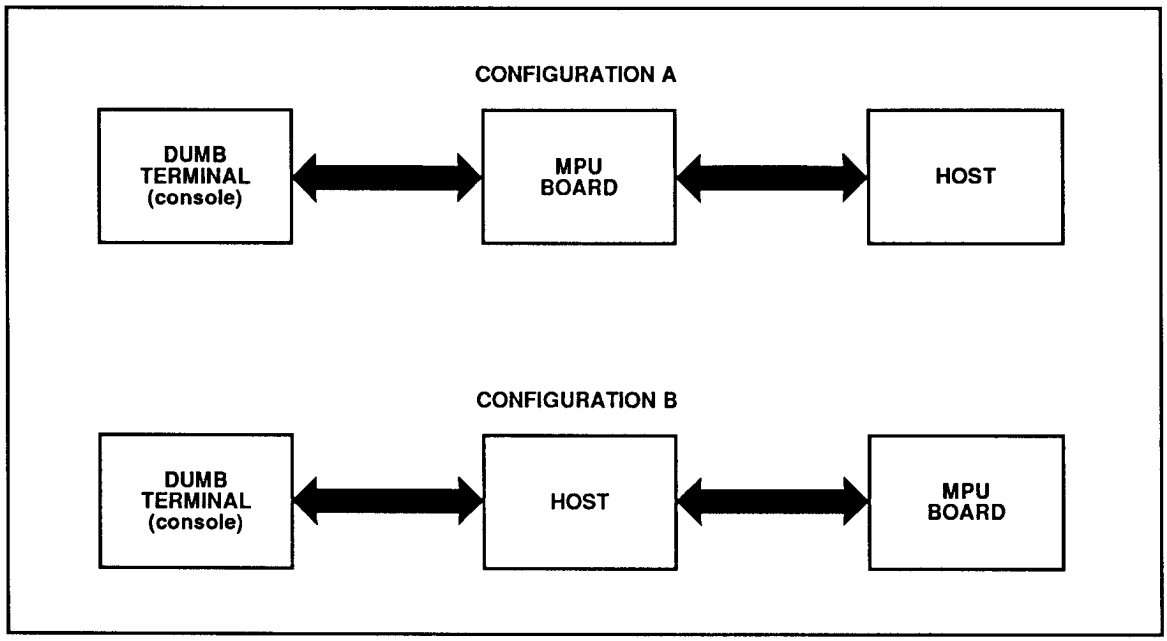

Figure A-1. Test Monitor communication configurations.

In the case of Configuration B, two conditions must be met:

1. The host must have the capability to act as a transparent terminal.

2. Download and host commands should be redirected to PORT1 by simply using the same drivers for both ports.

NOTE

The Test Monitor communicates with only the selected port. Thus, even though two RS232 ports can be connected, the ALTERNATE command must be used to select between connected communication devices.

ENTERING THE TEST MONITOR

The Test Monitor is entered through exceptions. The easiest way is through the NMI vector (vector #31). The NMI vector is entered by momentarily shorting pins 1 and 2 of J560 (see Figure 7-2 for location) on the MPU board. A **TRAP #F** instruction will also put you into the Monitor. In short, any exception not directly used by the system code can be used to enter the Monitor. However, the most likely exceptions will be vectors #2-31. A system error (such as a bus or address error) invokes the Test Monitor.

COMMAND CONVENTIONS

Syntax

When the Test Monitor is ready for a command input, it displays the prompt character

>

Commands consists of an ASCII character string terminated by a carriage return. For the sake of simplicity, command descriptions do not show the carriage return.

NOTE

You can perform in-line editing of the command string using either Control-H or RUBOUT as "erase previous character."

Identifying Process and Exchanges

Some Monitor commands require that you specify a process or an exchange. The syntax for identifying a process or an exchange is:

<process>name
<exchange>name

If a name is entered, the Monitor searches for the name and immediately converts it to an id. In either case, the Monitor requires that the identified process or exchange exist. An example is:

ROOT /*process or exchange named ROOT */

NOTE

Only exchange or process names use both shifted and non-shifted characters.

Ranges

Several Monitor commands require that you enter a memory address range. The syntax for entering an address range is:

<start> ::= <address>
<end> ::= <address>

That is, you can enter either a starting and ending address, or simply a starting address.

If you only enter a starting address, then a default ending address is generated and data will be displayed in byte mode. The value of the ending address is dependent on the command. Some commands require that you specify the ending address. This fact is noted in the command descriptions that follow.
In all cases, the address range specified is inclusive of both the starting and ending addresses. For example:

from address 1000 to address 10FF /* range from 1000_{16} to $10FF_{16}$ inclusive */

NOTE

All addresses are entered as an hexadecimal number.

Sizes

Some commands that operate on memory, require that you specify the size of the data element. The size must be one of the following:

B	Byte
W	Word (2 bytes)
L	Long (4 bytes)

If you omit "size" on a command that requires it, the 'B" (one byte) is used as default.

Patch Limiters

Patch commands operate in an interactive mode. These commands display an element and then they allow you to optionally change the value of the element. You must end each response you enter with a terminating delimiter (patch delimiter). This determines the nature of the next prompt. Delimiters are single characters:

.	Period terminates the command
CR	Carriage Return advances to the next element
BS	Backs up to the previous element

Patch delimiters, except CR and BS, must be terminated by a carriage return.

Displayed Values

Values are displayed in hexadecimal. For example:

```
00001234
```

Names

When the Test Monitor prints the name of a process or an exchange, it first checks to see if the name (32-bits) contains any non-printing characters. If so, then the name is printed as a 32-bit hexadecimal number. Otherwise, it is printed as a string, enclosed in single quotation marks. For example:

```
   'ROOT'
01020304
```

Error Messages

The following is a brief description of error messages produced by the Test Monitor.

"Unknown Command" Unable to pars the command lines as entered.

"Non-Existent or Inactive Process" You have entered a process name which does not exist.

"Non-Existent or Inactive Exchange" You have entered an exchange name which does not exist.

"Ending Address < Starting Address" You have entered an illegal memory range. Possibilities are:

- The ending address is less than the starting address
- Invalid (add) memory address
- The range does not begin or end on a WORD or LONG boundary when required to do so by the command or size operand you have entered.

"Break Table Full" You are attempting to define more than five breaks.

"Illegal Function" The function number you entered on a Kernel call or an IO call break is not defined in pSOS.

"Bad Address" You have entered an illegal address. This error results both when the Test Monitor detects an illegal input address, and when a BUS/ADDRESS error occurs in Test Monitor mode which is caused by erroneous user input (odd address, for example).

"No Process Information Available, Operating System not Initialized" You have entered a restricted command while in stand-alone mode.

COMMAND DESCRIPTIONS

As stated in the introduction, there are two versions of the Test Monitor; a RAM version and a RAM-less version. This gives the technician greater testing functionality and versatility.

RAM-Dependent Tests

These tests use system RAM when performing their tested functions. There are 16 RAM-dependent functions; namely, Clear Breakpoints, Display Breakpoints, Set Breakpoints, Dump Registers, Dump Memory, Fill Memory, Trace, Continue Execution, Boot, Disassembly, Set Registers, Transparent Mode (Host), Query Process, Query Exchange, Query Memory, and pSOS Service Calls. The following describes the functions and operation of each RAM-dependent test.

NOTE

RAM-dependent tests require fully functional DRAM in order to test their designed functions.

Test: **CLEAR BREAKPOINTS**

This command can be used to clear one or all breakpoints from the break table. Here you enter the characters BKC followed by a carriage return. The Test Monitor responds, prompting you for a breakpoint number 0 - 4, or all.

An example of the Clear Breakpoint command is:

>BKC
Breakpoint # = 0 (breakpoint number can be 0, 1, 2, 3, 4, or ALL)

Note that 0 = clear one breakpoint.

Test: DISPLAY BREAKPOINTS

This command is used to display the definitions of all currently defined breaks. To display breakpoints, enter the following command string:

BKD

All breakpoints will be displayed. The command display is self-explanatory.

Example of the Display Breakpoints command is:

```
>BKD
  BKPT OO 05843E
  BKPT 01 067342
  BKPT 02 003466
  BKPT 03 008532
  BKPT 04 0DE48A
```

Test: SET BREAKPOINTS

This command defines breakpoints. Up to five breakpoints can be defined and in place at a given time.

To set breakpoints, enter the following series of command strings:

BKS
<breakpoint number>
<breakpoint address>

Execution is halted prior to execution of the instruction at the specified address.

NOTE

These are software breakpoints and can only be placed in RAM. An error results if you try to set a breakpoint at a hardware address.

An example of the Set Breakpoint command is:

```
>BKS
  Breakpoint # = 0 (breakpoint number can be 0, 1, 2, 3, or 4)
  Address = F302
```

Test: DUMP REGISTERS

This command is used to display the saved processor registers. To dump user registers, enter the following:

DR

All current register status will be displayed.

The instruction field represents the Test Monitor's best effort at disassembling the memory content at the address pointed to by the PC. Depending on the microprocessor's mode, either USP (user stack) or SSP (supervisor stack) will have the same content as A7.

An example of the Dump Register command is:

```
>DR
-----Register Contents-----
```

Test: DUMP MEMORY

This command is used to display memory. If no ending address is entered, 80 bytes are displayed. To dump (display) memory, enter the following:

D

When prompted, enter the beginning address followed by a carriage return.

You will then be prompted for the ending address. Enter the ending address (followed by a carriage return).

Dump memory can be continued by simply pressing carriage return. In this case, each such continuation inherits the size and number of display elements from the original Dump Memory command.

An example of the Dump Memory command is:

```
>D
-------dump memory-------
from address    = 3000
to address      = 3030W
```

NOTE

You can specify whether you want the ending (dump) format in WORDS, or LONGS by terminating the ending address with a W (16-bit) or an L (32-bit) , respectively. The default is B (bytes).

The Dump Memory displays an integral multiple of 16 bytes, regardless the specified address range. This could cause problems when displaying memory with "holes" in the address range (such as is typical in examining peripheral hardware registers). The "holes" (non-existent locations) may cause bus error exceptions. In such cases, use the Patch Memory (P) command to display/alter memory.

Test: FILL MEMORY

This command is used to fill a memory range with a specified value. To fill memory, enter the following:

FM

When prompted, enter the beginning address followed by a carriage return.

Then, when prompted once again, enter the ending address followed by a carriage return. The ending address with (range) must be specified because the Fill Memory command will not provide a default. The <range> and <value> must agree with the defined <size>.

Finally, you are prompted for the data you want filled into memory. Enter (type in) the desired data pattern followed by a carriage return.

An example of the FM command is as follows:

```
>FM
-------fill memory-------
from address    = F500
to address      = F510L
fill value      = 00004F4B
```

NOTE

You can specify whether you want the fill format in WORDS or LONGS by terminating the ending address with a W or L; respectively. The default is B (bytes).

Test: TRACE

This command is used to execute one or more instruction steps. To trace an instruction, enter the following:

T

This action executes one instruction of the user program and displays the contents of the microprocessor's registers. You can continue this command to the next instruction by simply pressing the carriage return. At each step, the PC, hexadecimal object code, and mnemonic interpretation of the instruction executed is displayed. After each step, the standard breakpoint register display is shown.

An example of the T command is as follows:

```
>T
program interrupted--TRACE--

----contents of processor's registers----
```

Test: CONTINUE EXECUTION

This command is used to return to the application mode. The context of the suspended application is restored from the saved processor registers and control is returned to the application.

If <new PC> is entered, then the PC register will be loaded with <new address prior to execution. Otherwise, execution resumes at the save PC address.

To continue execution, enter the following:

GO

This causes processor control to return to the application software.

An example of the Continue Execution command is as follows:

```
>GO
```

Test: BOOT

To boot the system, enter the following:

BOOT

This starts the boot of the operating system without running kernel diagnostics. This command clears any breakpoints that were previously set.

Test: SET REGISTERS

To set registers, enter the following:

SR

You are then prompted for the address name (the address name is the same name as the name displayed in the Dump Register command). Finally, you are prompted for the value to which you wish to set the register.

Test: DISASSEMBLY

To disassemble memory, enter the following:

DI

You are then prompted for an address from which to begin disassembly.

Test: HOST

This command is used to invoke "transparent" mode. Enter the following:

HO

When in transparent mode, data input from one RS-232C port will be output to the other RS-232C port (This is possible when an RS-232 COMM pack is installed in the COMM pack slot and both the COMM pack and Host RS232 ports are connected to RS232 devices. The output port is configured as follows: 19,200 baud, no parity, 8-bits per characters.

The following example shows how the HOST command works:

> If a terminal is connected to the 1200C01 COMM pack port, the output port (host port) is the rear panel RS-232-C port. If the terminal is connected to the rear panel RS232 port, then the output port (host port) is the 1200C01 COMM pack port.

To terminate from host mode, press "CTRL]."

Test: QUERY PROCESS

This command is used to obtain general information about groups of processes, or to obtain detailed information about a single process.

To begin the query process, enter the following:

QP

The Test Monitor then prompts you for a process name. You have two choices:

1. If you want to query a specific process, enter the name of the process, followed by a carriage return. Information for the named process is then displayed.

2. If you want to query all processes, simply enter a carriage return following the Test Monitor's prompt for a process name.

If you want to query all processes, the order of the display is in reverse chronological order; that is, the most recent process is displayed first.

Displayed information is self-explanatory. However, the STATE information can be one of the following:

RUNNING	= last running process
MWAIT	= waiting for memory
XWAIT	= waiting for a message
VWAIT	= waiting for events
PAUSED	= paused
SUSPENDED	= suspended

If the process is waiting for memory, the size and region is displayed. If the process is waiting for a message, the XID is displayed. If a process is waiting for an event, the events are shown.

A "YES" in the "Susp?" column indicates that a process is suspended. If the process is in a WAIT state and is additionally suspended, then the WAIT status is shown. If the WAIT condition is removed, it will then show SUSPENDED.

A "YES" in the "TIMEOUT" column indicates that an optional time-out is in force.

An example of the Query Process command is:

>QP
Process name

NOTE

The processes displayed depend on whether you selected a single process or all processes. If a specific process is named, then a more detailed description of the state of the specified process is given. This additional information is mostly self-explanatory.

Test: QUERY EXCHANGE

This command displays either general information about all ACTIVE exchanges in the system, or detailed information about a specific exchange.

To begin a query exchange, enter the following:

QX

The Test Monitor then prompts you for an exchange name. You have two choices:

1. If you want to query a specific exchange, then enter the name of the exchange, followed by a carriage return. Detailed information about the name exchange is displayed.

2. If you want to query all exchanges, simply enter a carriage return following the Test Monitor's prompt for an exchange name.

If an exchange is specified, then the contents of the exchange's process-wait or its message-posted queue is also displayed. These queues are displayed with their elements in the order they appear in the queue. Otherwise, the display is fairly self-explanatory.

If you query all exchanges, then information on all "active" exchanges is displayed. The order of display is in reverse chronological order; that is, the most recent exchange is displayed first. Most fields in the display are self-explanatory. The "Max" field displays the maximum allowable length of the exchange's message queue. NONE indicates no limit.

An example of a Query Exchange command is

```
>QX
  Exchange Name
```

NOTE

Exchange information displayed depends on whether you selected a single exchange or all changes

Test: QUERY MEMORY

This command displays the current state of the pSOS memory manager. The size and region of each free memory segment is displayed. Also, the contents of the memory wait queue is displayed.

To begin a query memory process, enter the following:

QM

This displays the memory usage of the system.

An example of the Query Memory command is:

>QM

A display of memory usage appears

Test: pSOS SERVICE CALLS

The Service Calls command is used to issue kernel calls to pSOS while in the Test Monitor mode. Due to internal limitations, only a few kernel calls are allowed.

To initiate a pSOS service call, enter the following:

SC

The Test Monitor then displays a service menu and prompts you for the call you wish to perform. Enter (type in) the appropriate process or exchange name (found by using the QUERY PROCESS or QUERY EXCHANGE command).

Some Service Calls need more input data than others. In these cases, the Test Monitor prompts you as required. For example, **SU_P** (**SU**spend **P**rocess) requires only the process name; whereas, **SI_V** (**SI**gnal) requires the process name as well as the "signal in" Some processes may wait for a signal before continuing execution (signals are four-digit hexadecimal numbers). Example: An input/output driver may be waiting for a signal. When the Interrupt Service Routine gets a character, it sends a signal to the input/output driver to continue.

All Service Calls return a "return code." A return code of 00 means that the Service Call performed has no errors.

An example of the Service Call command is:

>SC

The Test Monitor displays Service Call Menu

RAM-Independent Functions

The following functions do not use system RAM in order to perform the commanded function. There are 13 RAM-independent functions. Eleven of them can be used to verify the functionality of system DRAM. These are: Patch Memory, Memory Size, Input from Port, Output to Port, Alternate Console, Read Scope Loop, Write Scope Loop, Refresh, Soak, ReSET System, and RAM Address Independence. Two functions can be used to check the functionality of Video Display RAM. These tests are: Display RAM Data Independence and Display RAM Address Independence.

Test: PATCH MEMORY

This command is used to interactively view and modify memory locations. To patch memory enter the following

P

The Test Monitor then prompts you for an address. Enter the address followed by a carriage return. If you want to patch words, or long words, terminate the patch address with a "W" or "L," respectively.

To move forward in memory, press the RETURN key. To move backward in memory, press the BACKSPACE key.

NOTE

If you try "to patch" a memory address that does not generate a DTACK signal, the message "BAD ADDRESS" is displayed.

An example of the Patch Memory command is:

```
>P
  address = F000
```

Test: MEMORY SIZE

This command is used to test memory size. To test memory size, enter:

M

The memory size test begins to run and the message "TESTING RAM" is displayed. When the test is done, the last good tested address is displayed: $1FFFFF_{16}$ bytes for the 2 Mbyte RAM version of the MPU board or $3FFFFF_{16}$ bytes for the 4 Mbyte RAM version of the MPU board.

Test: INPUT FROM PORT

This command allows you to input data from one of the selected communication ports. To input data from a port, enter the following:

I

The Test Monitor then prompts you for a port number. (Port 0 is the RS232 Port located on the rear of the MPU board; Port 1 is the keyboard port, and Port 2 is the 1200C01 COMM pack port.) Enter the desired port number followed by a carriage return.

Each time you press the RETURN key, the selected port is read, and the value read is displayed. Press the "." (period) key to terminate the input program.

Test: OUTPUT TO PORT

This command allows you to output data from the terminal console to the MPU board via one of the RS-232C communication ports. To output data to an MPU communication port, enter:

O

The Test Monitor then prompts you for a port number. Port 0 is the local RS232 port; Port 1 is the keyboard port; and Port 3 is the 1200C01 COMM pack port. Enter the desired Port number followed by a carriage return.

The Monitor then displays the address of the Port to which you wish to write. Now, enter the value you want written to that port. Every keystroke will be written to the specified port. The only character not sent will be the "." (period). Use the period to terminate the output command.

Test: ALTERNATE CONSOLE

This command allows you to switch between two connected RS232 ports. To switch between RS-232C ports, enter the following:

A

Communication is now via the alternate RS-232C port. For example, Ports 0 and 2 may each be connected to a terminal console. However, the Test Monitor can only communicate with one console at-a-time via the selected port. This command simply allows you to use a selected console for a special purpose.

Test: READ SCOPE LOOP

This command continually reads a specified address byte or word. A scope or logic analyzer can be attached at key circuit points for low-level troubleshooting and analysis. To initiate a Read Scope Loop, enter:

R

The Test Monitor now prompts you for an address that you wish to read (only bytes and words are allowed). If you want to read words, terminate the address with a "W." Bytes are the default.

Following the carriage return, the Test Monitor displays both the address that is read and the the data that was read from the addressed location.

Press any key to terminate the Read Scope Loop command.

Test: WRITE SCOPE LOOP

This command continually writes specified data to a specified memory address. A scope or logic analyzer can be attached at key circuit points for low-level troubleshooting and analysis. To initiate a Write Scope Loop, enter:

W

The Test Monitor now prompts you for an address to which you want to write and for data to write into memory (only bytes and words are allowed). If you want to write words, terminate the address with a "W." Bytes are the default.

Following the carriage return you entered for the last prompted data, the address that is written to is displayed, as well as the data that was written to the addressed location.

Press any key to terminate the Write Scope Loop command.

Test: REFRESH

This command allows you to test the RAM refresh circuitry. To initiate the test, enter the alpha characters

RT

The Test Monitor then prompts you for the number of seconds you wish to wait for any refresh errors. Enter the number of seconds in hexadecimal. The minimum number is one second; the maximum is $7E90_{16}$ or $32{,}400_{10}$ seconds.

Test: RAM SOAK

This command allows you to test the RAM cell integrity. To initiate the test, enter the alpha characters

ST

The Test Monitor then prompts you for the number of seconds you wish to wait for any soak errors. Enter the number of seconds in hexadecimal. The minimum number is one second; the maximum is $7E90_{16}$ or $32{,}400_{10}$ seconds

Test: RESET SYSTEM

This command can be used to reset the system. To reset the system, enter the alpha characters:

RSET

This performs a software reset of the system and starts executing code as if a hard reset or a power-up reset was performed.

Test: RAM ADDRESS INDEPENDENCE

This test allows you to identify addressed lines that may be shorted, held high, or held low. To start the RAM Address Independence test, enter the alpha characters:

RAT

If the test passes, a "pass message" is displayed. If the test fails, the following data is displayed.

- The base address (the address in which the test started)
- The failure structure
- The expected and actual data read

From the information contained in the base and failure address, you should be able to determine which address lines are shorted, held high, or held low.

The following RAM locations tested are:

0000 0001 0002 0004 0008 0010 0020 0040 0080 0100 0200 0400 0800
1000 2000 3000 4000 10000 20000 40000 80000

This test saves the RAM locations tested in the graphics RAM (graphics RAM is part of video RAM).

RAM locations are written with 0000. The first location is checked for zero; if zero, then FFFF is written. The subsequent locations are then checked to verify that they still contain zero. The next address (0001) is written with FFFF (now address 0001 becomes the base address) and the subsequent addresses are checked again to verify that they still contain zero. This sequence continues until all tested addresses have been written with FFFF.

If a failure occurs, the test aborts and the failure information is displayed. The base address is the last address that was written with FFFF. The failure address is the address that expected to read 0000, and instead read a different value. For example:

```
Base Address  = 00000002
Address       = 00000008
Expected      = 0000
Actual        = FFFF
```

In the preceding example, address 00000002 is shorted to address 00000008 (address lines KA1 and KA2 are shorted). Therefore, writing FFFF to address 00000002 appears to write to address 00000008 as well.

Test: DISPLAY RAM DATA INDEPENDENCE

This test allows you to identify display RAM addressed lines that may be shorted, held high, or held low. To start the Display RAM Data Independence test, enter the alpha characters:

DRDT

If the test passes, a "pass message" is displayed. If the test fails, then failure information is printed on the console screen.

This test sets each long word in display RAM to $00000000. The first location of RAM is then checked to see if it contains 0000. Each bit, one bit at a time, is asserted high and checked by reading that word. For example, 0001 is written to Display RAM and the same location is read to check for the written value. . . 0002 is written and checked in the same way. . . then 0004, 0008, 0010, 0020, 0040, 0100, 0200, 0400, 0800, 1000, 2000, 4000, 8000. After each write, RAM is read and checked. If an error is detected, a failure message is displayed on the console screen. For example:

```
Address   = 00000000
Expected  = 0020
Actual    = 0030
```

In this example, data bits 4 and 5 appear to be shorted to each other.

Test: DISPLAY RAM ADDRESS INDEPENDENCE

This tests allows you to test the address decoding and cell integrity of display RAM. To start the Display RAM Address Independence test, enter the alpha characters:

DRAT

If the test passes, a "pass message" is displayed. If the test fails, then failure information is printed on the console screen.

Each long word in display RAM is set to $55555555 and then set to $AAAAAAAA. The test then checks that RAM was set to $AAAAAAAA.

All long words in display RAM remain set to $AAAAAAAA.

Test: DISPLAY RAM ADDRESS INDEPENDENCE

This tests allows you to test the address decoding and cell integrity of display RAM. To start the Display RAM Address Independence test, enter the alpha characters:

DRAT

If the test passes, a "pass message" is displayed. If the test fails, then failure information is printed on the console screen.

Each long word in display RAM is set to $55555555 and then set to $AAAAAAAA. The test then checks that RAM was set to $AAAAAAAA.

All long words in display RAM remain set to $AAAAAAAA.